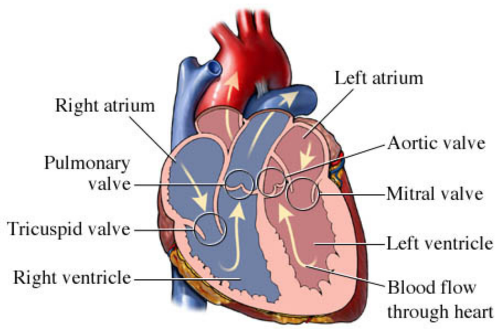
Module 1

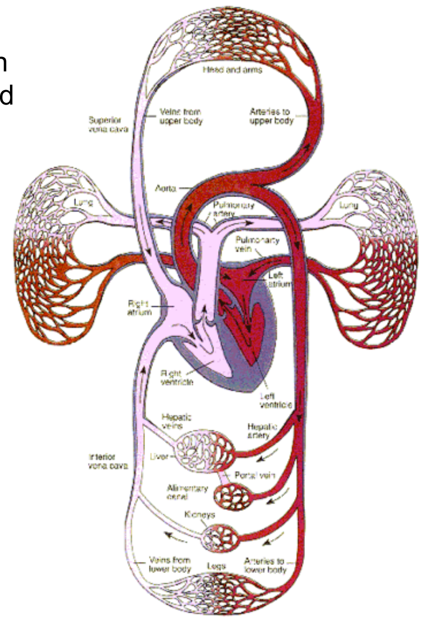
Semiconductor (*pn*-Junction) Diodes

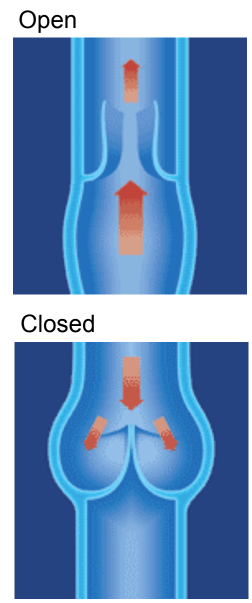
What are they and what is their purpose?

Diodes are electronic "check valves" which allow current to flow freely in one direction, but block current flow in the opposite directic

Essentially, they serve the same function in circuits, as the valves in your heart and veins do in your body.





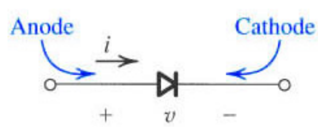


How do they work? (Module 2)

Semiconductor (*pn*-Junction) Diodes

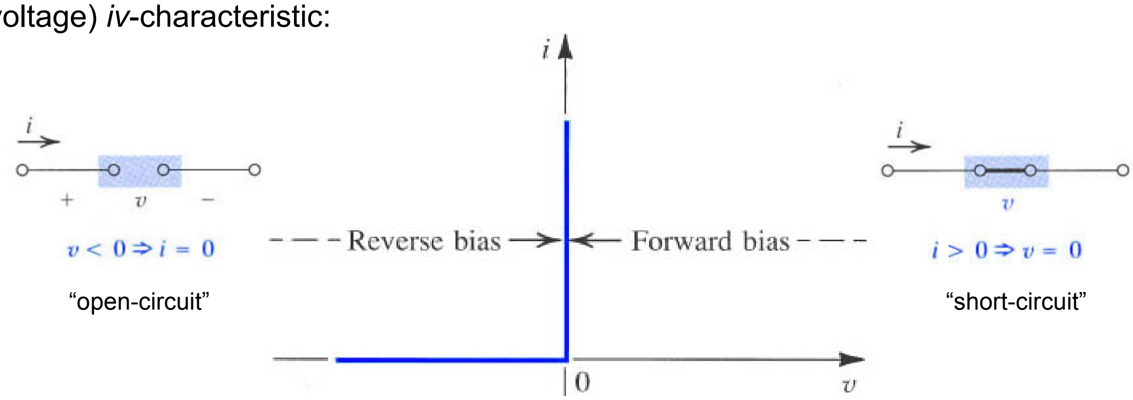
Physically, diodes are formed by the interface between two regions of oppositely doped semiconductor (*i.e.*, *pn* junction) and are thus, structurally, the simplest semiconductor devices used in electronics.

Circuit Symbol:



<u>Ideal Diode</u>

An *ideal diode* is a two-terminal device defined by the following non-linear (current-voltage) *iv*-characteristic:



Note: From the above, it follows that zero power dissipation occurs in an ideal diode!

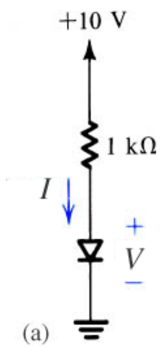
Forward Biased Regime (v > 0): Zero voltage drop occurs across a forward-biased ideal diode (*i.e.*, the diode behaves like an ideal short circuit).

Reverse Bias Regime (v ≤ 0): Zero current flows in a reverse-biased ideal diode (*i.e.*, the diode behaves like an <u>open</u> circuit).

➤ Determine the polarity of the voltage across the diode, then "replace" the diode with its equivalent circuit (either open-cct. or short cct.) and proceed with linear circuit analysis.

DC Behavior:

e.g. The diodes in each of the following circuits can be assumed to be ideal.

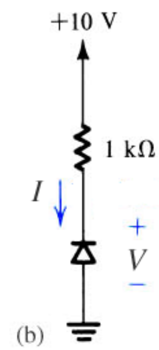


(a)

D Fwd. biased

$\therefore V = 0$

$$I = \frac{+10\text{ V} - 0\text{ V}}{1\text{ k}\Omega} = 10\text{ mA}$$



(b)

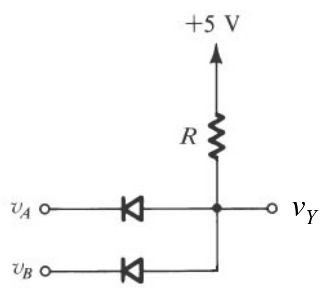
D Rev. biased

$\therefore I = 0$

$$V = +10\text{ V} - (0\ A)(1\text{ k}\Omega) = 10\text{ V}$$

e.g. The diodes in each of the following circuits can be assumed to be ideal, and the voltages v_A and v_B can be either +5 V or 0 V.

(a)

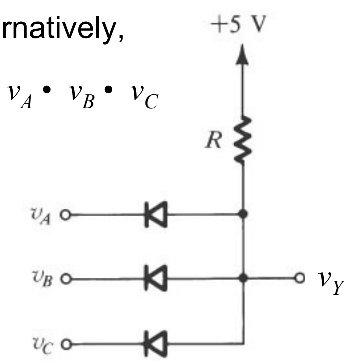


v_A	v_B	v_Y
0	0	0
0	5	0
5	0	0
5	5	5

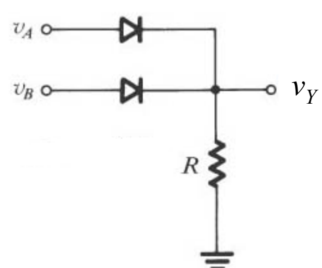
$v_Y = v_A \bullet v_B$ AND Gate

Alternatively,

$v_Y = v_A \bullet v_B \bullet v_C$

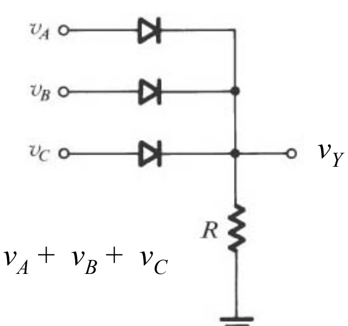


(b)



v_A	v_B	v_Y
0	0	0
0	5	5
5	0	5
5	5	5

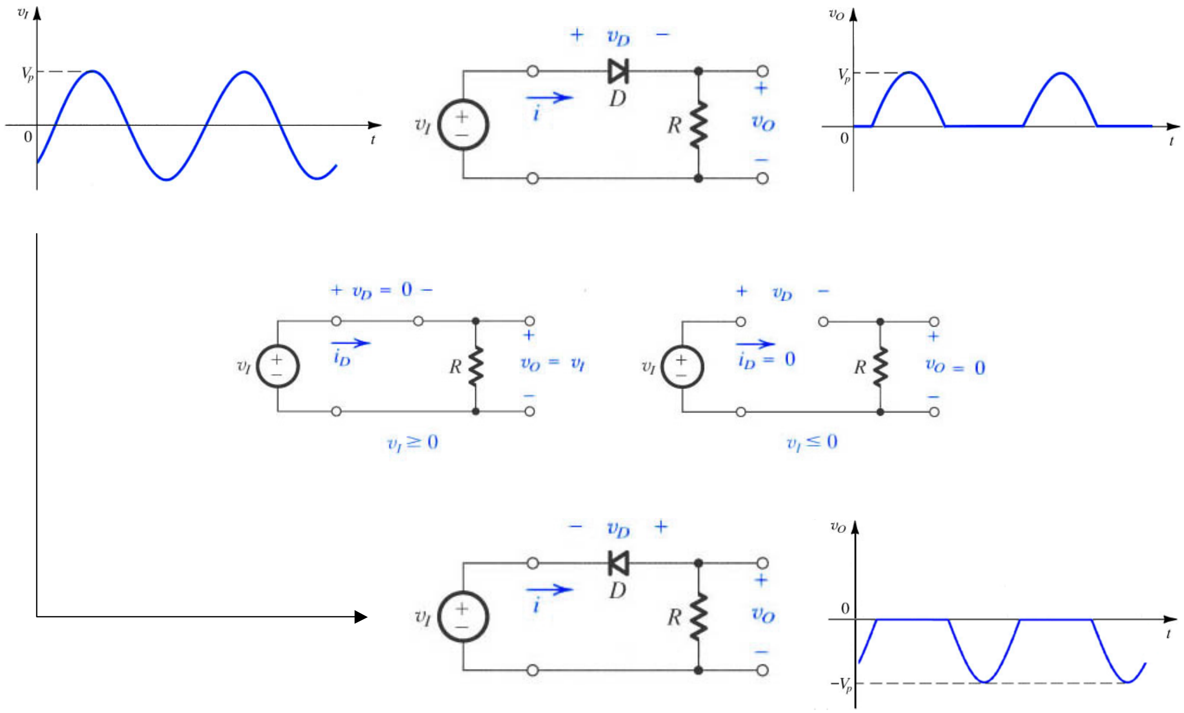
$v_Y = v_A + v_B$ OR Gate



$v_Y = v_A + v_B + v_C$

AC Behavior:

e.g. The diode in the following circuit can be assumed to be ideal.



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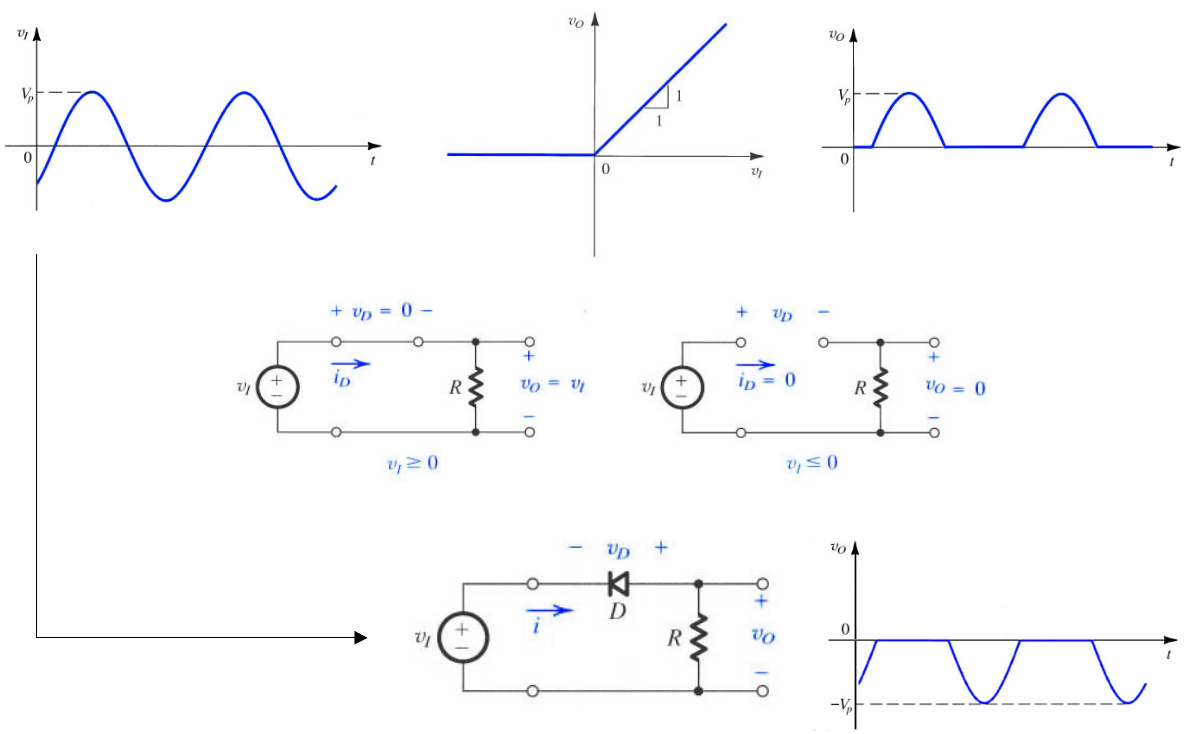

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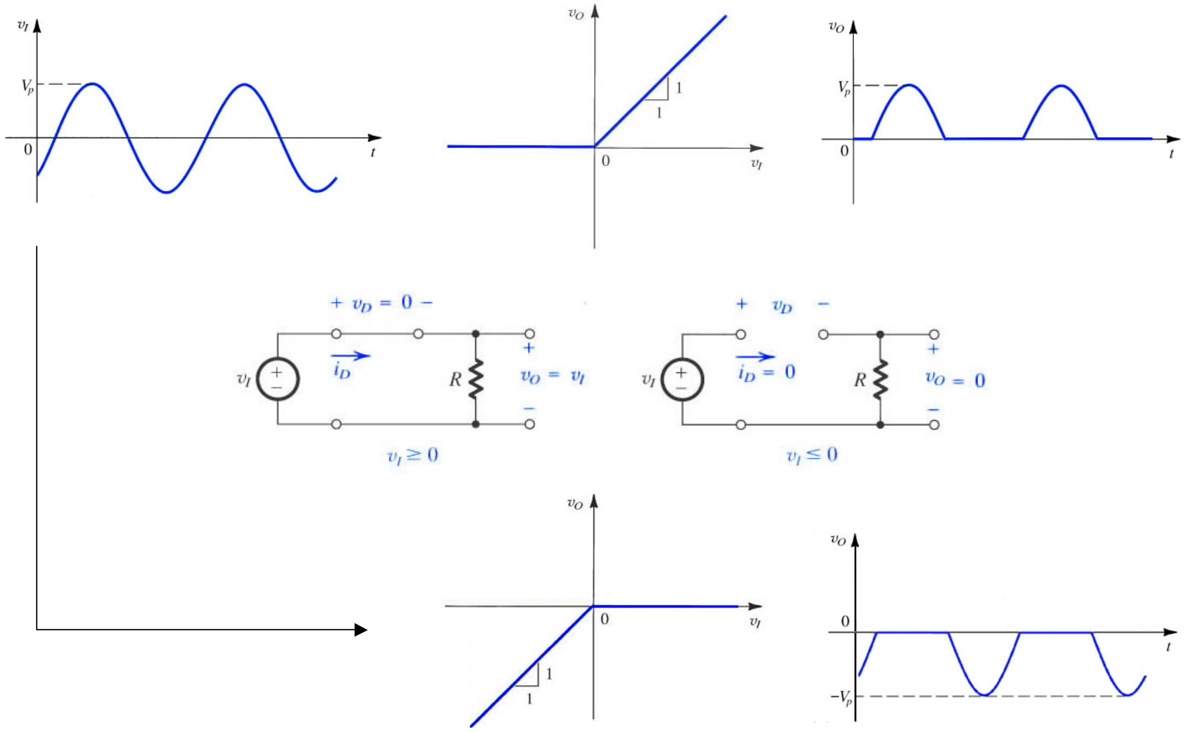
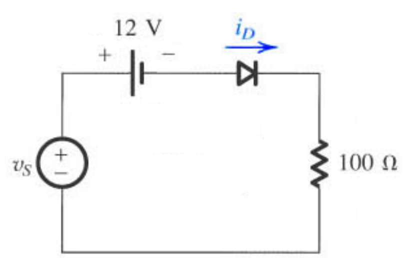
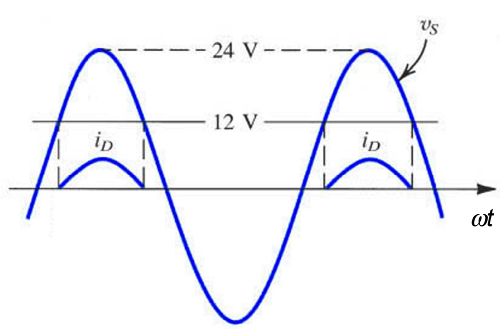


Conduction Angle:

Consider the current flowing in the following circuit where the diode is ideal and $v_S = 24\,sin(\omega t)$ V.

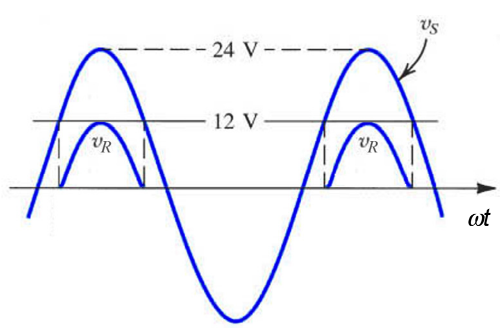




The diode begins to conduct when v_S = 12 V.

The voltage across the resistor has the same waveform as the current (i.e., remaining zero until v_S = 12 V). The amplitude (i.e., maximum) load voltage is thus

$V_R = V_S - 12\text{ V} = 24\text{ V} - 12\text{ V} = 12\text{ V}.$



Conduction Angle:

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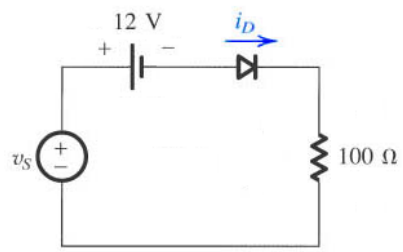
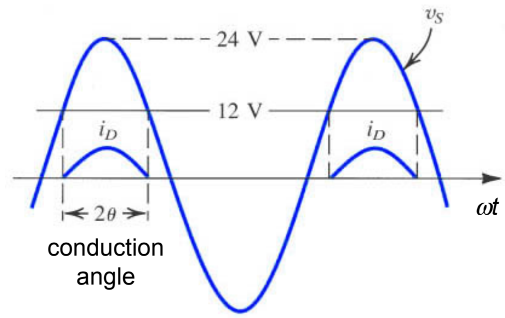




The diode begins to conduct when v_S = 12 V, which occurs at a phase angle defined by 24 $sin(\omega t)$=12 V. Or, in terms of the conduction 2θ as defined in the figure above,

$$24\,sin\left(\frac{\pi}{2}-\theta\right)=12\text{ V}$$

$$\text{or}\quad 24\,cos(\theta)=12\text{ V}$$

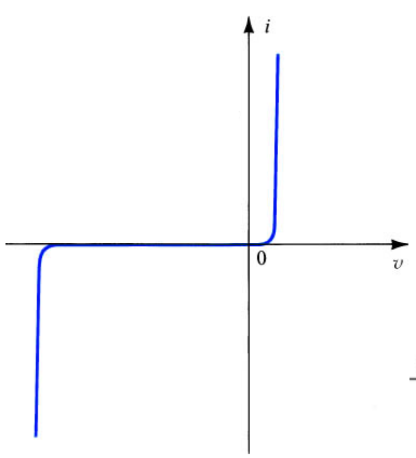
$$\therefore\quad 2\theta=2\,cos^{-1}\left(\frac{12\text{ V}}{24\text{ V}}\right)=120^\circ$$

The conduction angle characterizes the fraction of a period that the diode is "on".

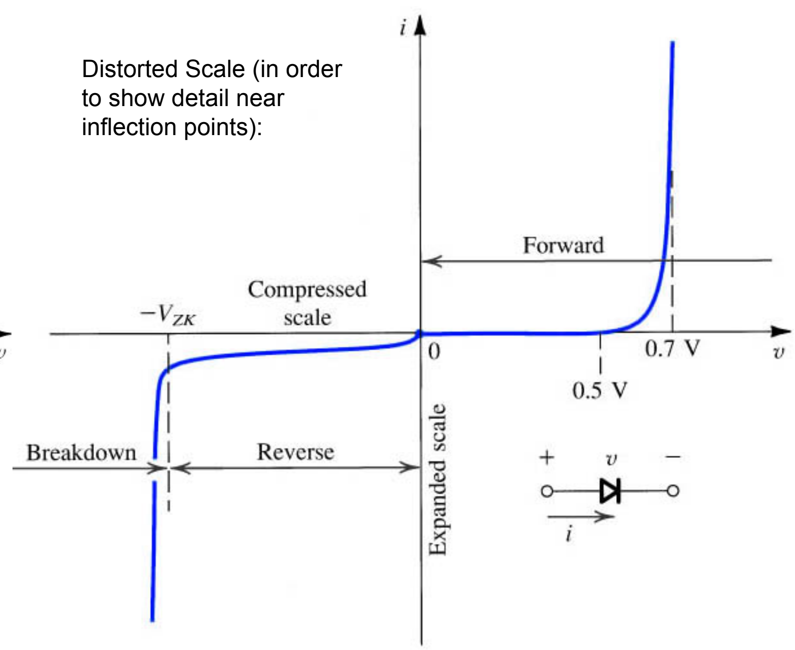
<u>Real Diode</u>

The physics of real *pn*-junctions leads to the following (non-ideal) *iv*-characteristic:

Realistic Scale:



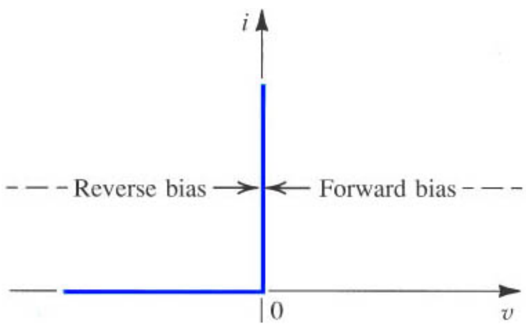
Distorted Scale (in order to show detail near inflection points):

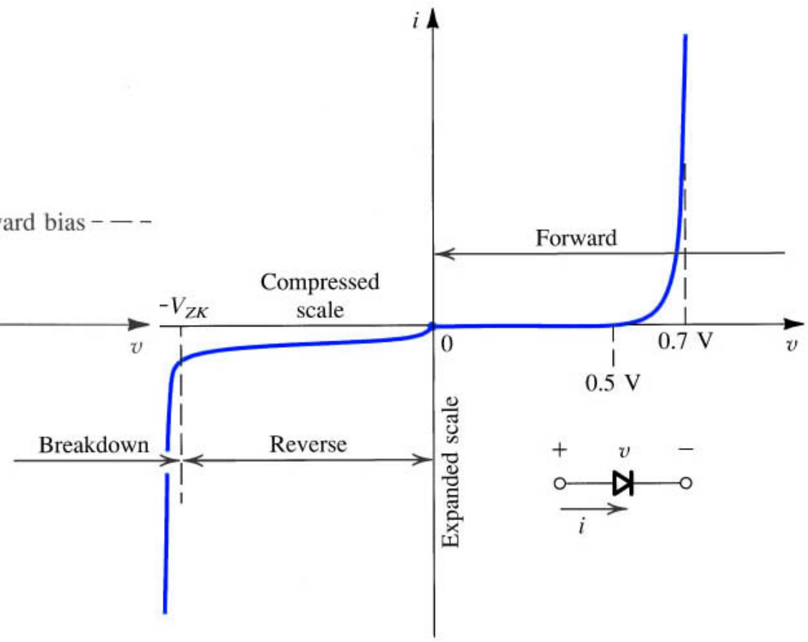


Note that real diodes exhibit three distinct operating regions (*cf*. two for the ideal diode)!

Compare...

Ideal Diode **Real Diode**





Forward (FWD) Bias Regime (v > 0):

The *iv*-characteristic in this region is closely approximated by the exponential relation,

$$i = I_S \left(e^{v/nV_T} - 1 \right) \qquad \text{"Diode Equation"}$$

where: I_S = *Reverse Saturation Current* (also called *Scale Current* in S&S text, since $I_S \propto A_{jctn}$). Typically, I_s is very small: pA for discrete silicon diodes, fA for integrated circuit diodes;

n = empirical constant (typically $1 \leq n \leq 2$, depending on the type of diode and its physical structure);

V_T = *Volt-Equivalent of Temperature* or *Thermal Voltage* defined by

$$V_T = kT/q$$

where: k = Boltzmann's constant (also written k_B) = $1.38\text{x}10^{-23}$ J/K;
T = Absolute Temperature (K);
q = Electronic Charge = 1.602×10^{-19} C.

e.g. At 20 °C, V_T = 25.2 mV ≈ 25 mV (used throughout S&S text and this course).

Clearly, for larger currents (where $i >> I_S$ or $v > 10\ nV_T$), the diode equation simplifies slightly to

$$i \cong I_S e^{v/nV_T}$$

which is the form most commonly used to describe forward-biased diode currents larger than a few μA.

Values of I_S and n are normally specified by the diode manufacturer. However, I_S and n can be determined empirically if 2 measured operating points (I_1, V_1) and (I_2, V_2), are available; if a reasonable estimate for n is available, then 1 measured operating point is sufficient. In this course, if n is not given (or not computable from available data), assume n=1.

Reverse (REV) Bias Regime ($-V_{ZK} \leq v \leq 0$):

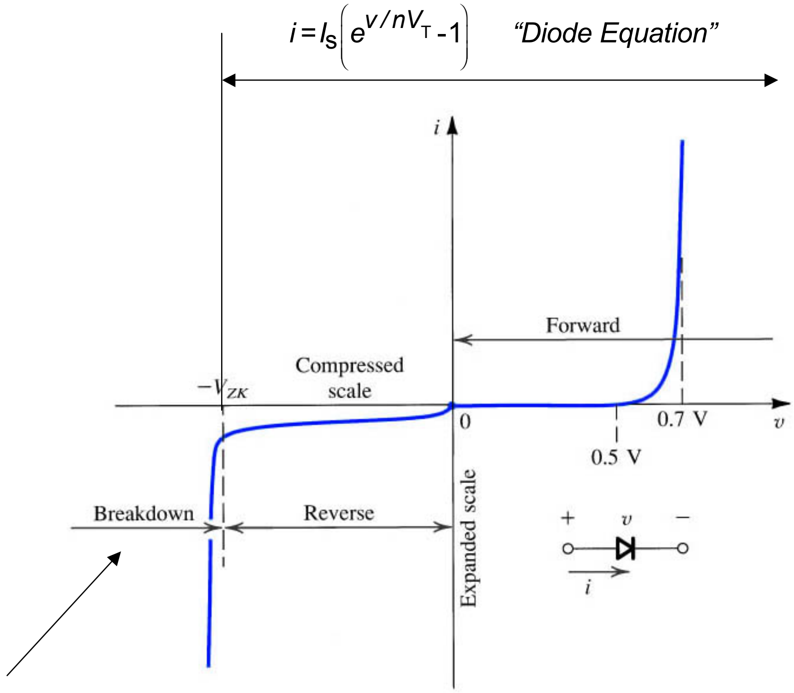
The reverse diode current is also described by $i = I_S\left(e^{v/nV_T} - 1\right)$, however, $e^{v/nV_T} \to 0$ when $v << 0$, thus the diode equation reduces to

$$i \approx -I_S$$

so the current "saturates" at $-I_S$ when the diode is significantly reverse biased (and hence the name *Reverse Saturation Current*).

The diode equation is valid throughout the *forward bias* and *reverse bias* regions of the *iv*-characteristic:

$$i = I_S\left(e^{v/nV_T} - 1\right) \quad \textit{"Diode Equation"}$$



In this region, the diode breaks down and so does the diode equation!

Breakdown (BKD) Regime ($v \leq -V_{ZK}$):

A reversible breakdown occurs when $v < -V_{ZK}$, which gives rise to the steep gradient in the *iv*-characteristic in this region.

There are actually two distinct breakdown mechanisms:

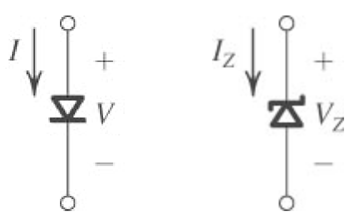
1. Zener breakdown (predominates if $-5 \leq -V_{ZK} \leq -2$ V) - *due to excess carriers generated by direct disruption of covalent bonds caused by extremely high E-field within depletion region of highly doped semiconductors;*
2. Avalanche Breakdown (predominates if $-V_{ZK} < -7$ V) - *due to excess carriers generated by collision-induced ionization in depletion region of lightly doped semiconductors.*

A combination of these mechanisms is usually responsible in diodes where $-7 \leq -V_{ZK} \leq -5$ V.

Typical diodes used in signal processing applications have $-V_{ZK} < -30$ V and are optimized for FWD or REV bias operation. However, some diodes are specifically designed for operation in the BKD regime. Diodes optimized for operation in the breakdown regime are typically called *Zener* diodes, regardless of which mechanism dominates.

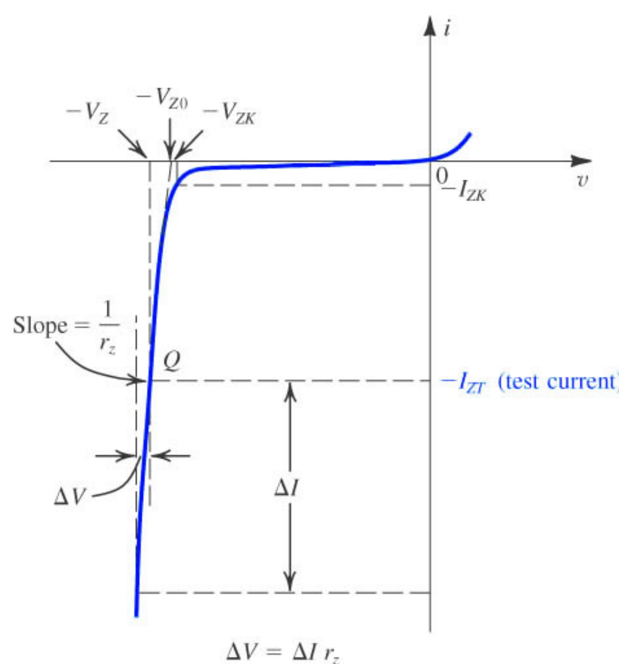
Detail of diode *iv*-characteristic in the breakdown regime:

All real diodes exhibit this behavior, but only Zener diodes are normally operated in the breakdown regime.



Signal Diode

Zener Diode

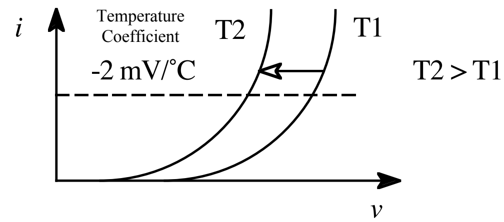


Note the opposite polarity convention compared to signal diodes (since Zener diodes are almost always reverse biased).

Note also that the current-voltage behavior of Zener diodes in the reverse bias and forward bias regimes is the same as for signal diodes.

Temperature Dependence:

Forward Bias Regime: At a given (constant) diode current, v exhibits an approximately linear shift in the *iv*-characteristic due to the combined effect of the temperature dependences of both I_S and V_T.



> Rule of Thumb: Typically, the *iv*-characteristic shifts approximately -2 mV/°C.

Reverse Bias Regime: The temperature dependence of the reverse current is that of I_S alone, which changes exponentially as a function of temperature.

> Rule of Thumb: Typically, I_S approx. doubles for every 10 °C increase in Temperature.

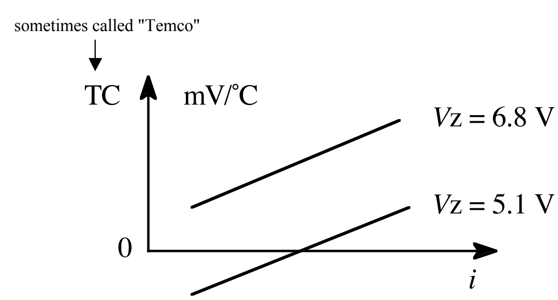
These variations may lead to significant changes in the operation of a circuit over a large temperature range and, in many applications, requires compensation strategies to be implemented in the design of some circuits.

In this course, unless stated otherwise, assume that the temperature remains constant at ~300 K (Room temperature).

Breakdown Regime: The *temperature coefficient* (TC) of Zener diodes depends on both voltage and current and, like in the FWD bias regime, leads to an approximately linear shift in the *iv*-characteristic.

In this regime, however, the TC > 0, at least over an appreciable range of currents.

e.g., A 6.8 V Zener diode exhibits a TC≈+2 mV/˚C, which is complementary to a forward biased diode!

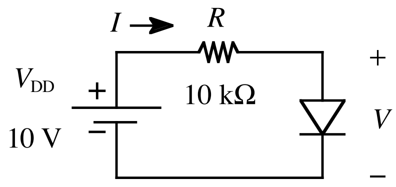


This leads to a popular strategy for compensating for the temperature dependence of Zener diodes depicted below:

Here, the diode current is nearly independent of T (over a useful range of i). Commercially available Zener diodes are often packaged in this configuration.

Analysis of Diode Circuits

e.g. Consider the following circuit where the diode is to be treated as real:

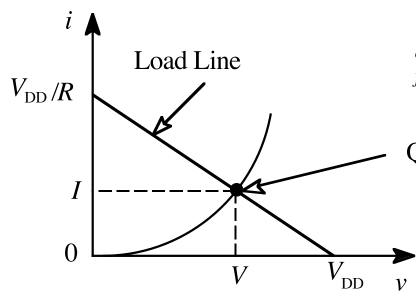


$$V_{DD} = IR + V \qquad (1)$$

$$I = I_S(e^{V/nV_T} - 1) \qquad (2)$$

Exact Solution: If I_S and n for the diode are known, then (1) and (2) can be solved simultaneously to obtain I and V.

Graphical Solution: If data are available, then (1) and (2) could be plotted and I and V could be obtained from the intersection.



a similar graphical method is used for the analysis of transistors - later

Approximate Solution: If an exact solution is not required, an approximation can be found using an <u>iterative</u> approach.

e.g. Suppose the diode is specified as exhibiting a 0.7 V drop at 1 mA (in the textbook, this is sometimes called “a 1-mA diode” for short), with n = 1.8.

step 0) Assume that the diode can be adequately described by $I \cong I_S e^{V/nV_T}$ (2 ')

Substitute I=1 mA and V=0.7 V (from specs.) to calculate I_S

$$I_S = 10^{-3} e^{-0.7/nV_T}$$

which yields

$$I = 10^{-3} e^{(V-0.7)/nV_T} \quad \text{or} \quad V = nV_T \, ln(I/10^{-3}) + 0.7 \qquad (2'')$$

step 1) As a first guess/approximation, assume V=0.7 V, then

$$I = \frac{V_{DD} - V}{R} = \frac{10\text{ V - }0.7\text{ V}}{10\text{ k}\Omega} = 0.93\text{ mA}$$

The accuracy can be improved by iterating between (1) and (2") as follows:

step 2) Substitute the value of I found in step 1 into (2") to calculate a new value for V

$$V = (1.8)(0.025)ln(0.93) + 0.7 = 696.7 \text{ mV}$$

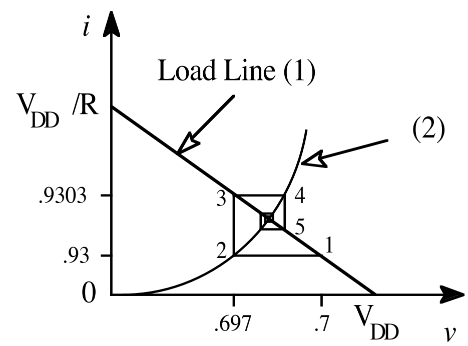
step 3) Substitute this value back into (1), to calculate a new value for I

$$I = \frac{10 \text{ V} - 0.697 \text{ V}}{10 \text{ k}\Omega} = 0.9303 \text{ mA}$$

step 4) Continue iterating between (1) and (2") until

$$\frac{(I_n - I_{n-1})}{I_n} \leq 1\% \qquad \text{(arbitrary precision)}$$

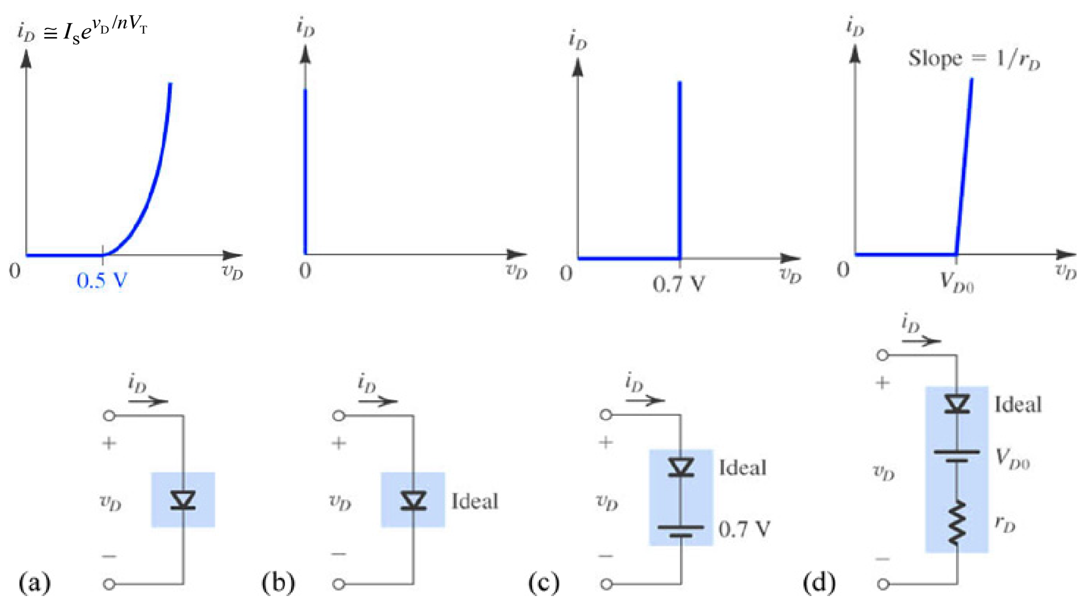
Graphical representation of iterative method:



Alternatively, appropriate simplifying assumptions can yield an approximate solution that, while not as accurate, may be good enough for many applications!

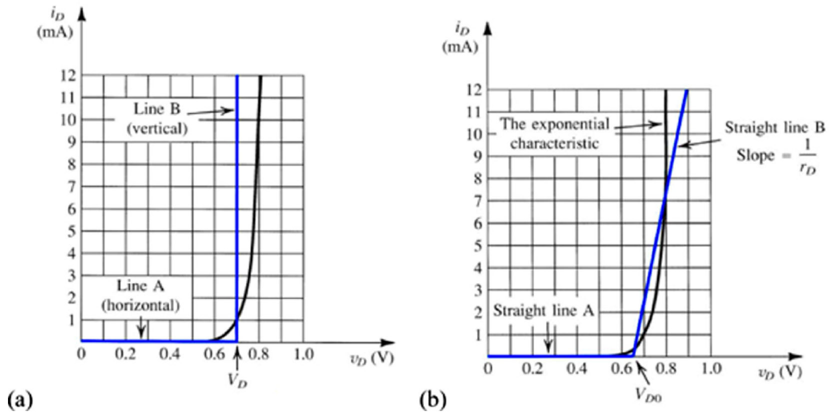
Recall: $i = I_S\left(e^{v/nV_T} - 1\right)$ *"Diode Equation"*

Large-Signal Diode Models (for approximate analyses):



The choice of which model to apply in a given design/analysis depends on the operating point of the diode and the magnitude of the other voltages and currents in the circuit.

Linearized (large-signal) models of the diode forward bias characteristics superimposed on an exponential real diode characteristic. (a) Constant-Voltage-Drop model; (b) Piecewise-Linear (“Battery-plus-Resistance”) model.



Simplified Exponential: Accurate if $i_D >> I_S$ (*e.g.*, >µA); useful for iterative analyses.

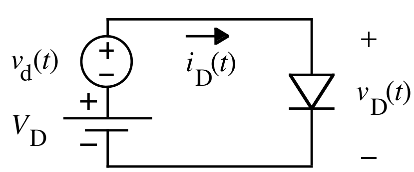
Ideal Diode: Adequate if v_D is small compared to other voltages in the circuit; also useful for qualitative analysis of circuit operation.

Constant-Voltage-Drop: Reasonable approximation at higher currents.

Piecewise-Linear: Reasonable approximation for “mid-range” currents (deviates rapidly at currents higher or lower than intersection points with true characteristic).

Small-Signal Diode Model:

Consider the following circuit:



total instantaneous voltage — quiescent DC voltage — AC voltage

$$v_D(t) = V_D + v_d(t)$$

$$i_D(t) = I_S\, e^{v_D(t)/nV_T}$$

The expression for $i_D(t)$ can be expanded in a Taylor series about the operating point to obtain

$$i_D(t) \approx I_D\left(1 + \frac{v_d(t)}{nV_T}\right) \quad \textit{Small-Signal} \quad \textit{Approximation}$$

$$\text{Recall: } f(x) = \frac{f(x_o)}{0!} + \frac{(x - x_o)}{1!} f'(x_o) + \frac{(x - x_o)^2}{2!} f''(x_o) + \cdots \quad \textit{Taylor's Series}$$

where $I_D = I_s e^{V_D/nV_T}$ = diode current when $v_d(t) \equiv 0$,

which remains a good approximation provided

$$\frac{v_d}{nV_T} << 1 \qquad (\textit{e.g.}, v_d < 10\text{mV at } 20\ ^\circ\text{C for a diode with n=2})$$

Thus, superimposed on the dc current I_D, is a small-signal ac current $i_d(t)$ such that

$$i_D(t)=I_D+i_d(t)$$

where

$$i_d(t)=\frac{I_D}{nV_T}v_d(t)$$

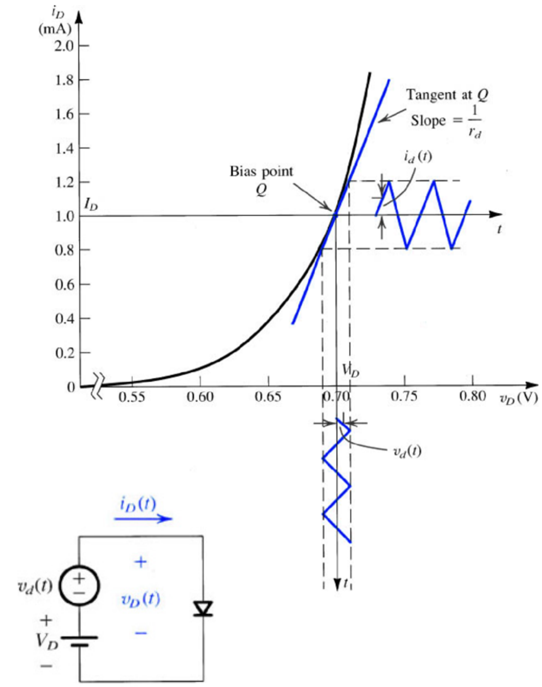
Notice that the term I_D/nV_T has the dimensions of conductance, and hence

$$g_d \equiv \frac{I_D}{nV_T} = \textit{Small-Signal Conductance}$$

or

$$r_d \equiv \frac{nV_T}{I_D} = \textit{Small-Signal Resistance}$$

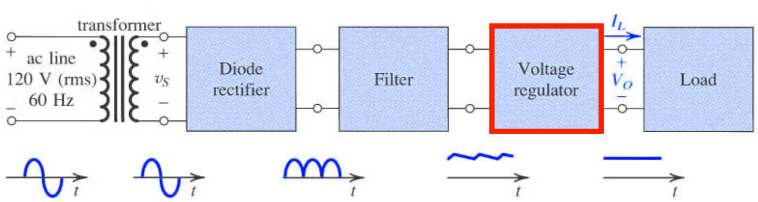
Sometimes r_d is also called the *Incremental Resistance*.



e.g., A voltage-controlled attenuator (see separate notes posted on WWW site).

Diode Applications: Power Supplies

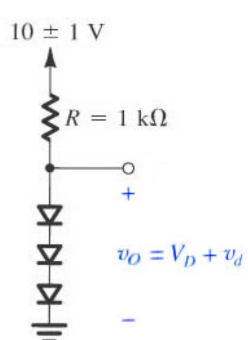
Consider the following DC power supply network:



Require a simple circuit that removes as much of the residual "ripple" as possible from a power supply.

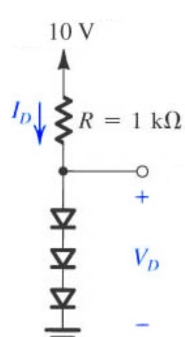
e.g., A simple diode "voltage regulator":

Consider the following circuit where each of the (identical) diodes are characterized by $V = 0.7$ V @ $I = 1$ mA and n = 2. Determine $v_O = V_D + v_d$ with no load ($R_L = \infty$).



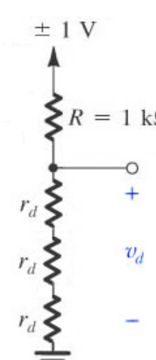
1

DC equiv. cct. →



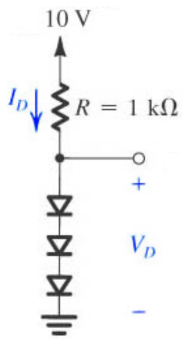
2

small-signal equiv. cct. →



Given that, for each diode, V = 0.7 V @ I = 1 mA and n = 2, I_S can be computed and V_D can be found using an iterative analysis:

1



DC equiv. cct.

$I_S = (1\text{ mA})e^{-(0.7\text{ V})/(2)(25\text{ mV})} = 8.3 \times 10^{-7}$ mA

Initial estimate for individual diode voltages, $V_D' = \sim 0.7$ V

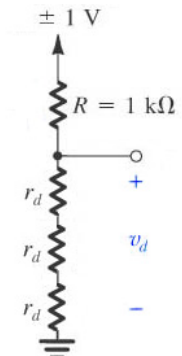
$$V_D = 3 \times (0.7\text{ V}) = 2.1\text{ V} \quad \rightarrow \quad I_D = \frac{10\text{V} - 2.1\text{V}}{1k\Omega} = 7.9\text{mA}$$

$$\text{new } V_D' = (2)(25\text{mV})\ln\left(\frac{7.9\text{mA}}{8.3\text{x}10^{-7}\text{mA}}\right) = 0.803\text{V}$$

$$V_D = 3 \times (0.803\text{ V}) = \mathbf{2.41\ V} \quad \rightarrow \quad I_D = \frac{10\text{V} - 2.41\text{V}}{1k\Omega} = \mathbf{7.59\ mA}$$

$$\text{new } V_D' = (2)(25\text{mV})\ln\left(\frac{7.59\text{mA}}{8.3\text{x}10^{-7}\text{mA}}\right) = 0.801\text{V}$$ (<1% change in V_D' so close enough)

2



small-signal equiv. cct.

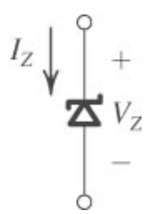
$$r_d = \frac{nV_T}{I_D} = \frac{(2)(25\text{ mV})}{7.59\text{ mA}} = \mathbf{6.59\ \Omega}$$

$$v_d = (\pm 1\text{V})\frac{3r_d}{R + 3r_d} = \mathbf{\pm 19.4\ mV}$$

$$\therefore \quad v_O = V_D + v_d = \mathbf{2.41\ V \pm 19.4\ mV} = 2.41\text{V} \pm 0.8\ \%$$

So the fluctuations in the output voltage have been reduced by ~10x compared to the input voltage!

Recall that the *iv*-characteristic of diodes operating in the breakdown regime is essentially linear!

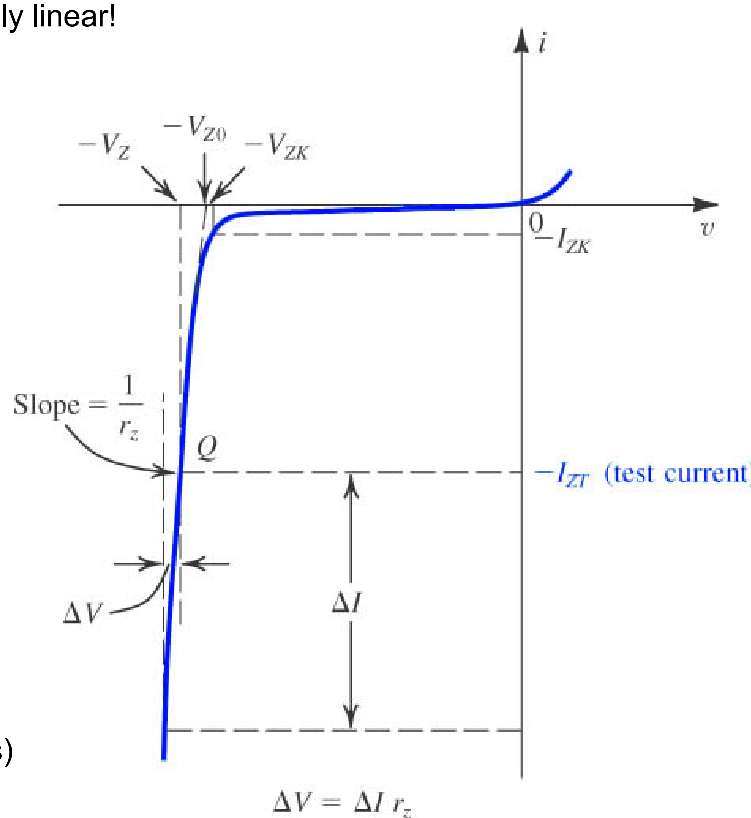


Zener Diode

$$V_Z = V_{Z0} + r_Z I_Z$$

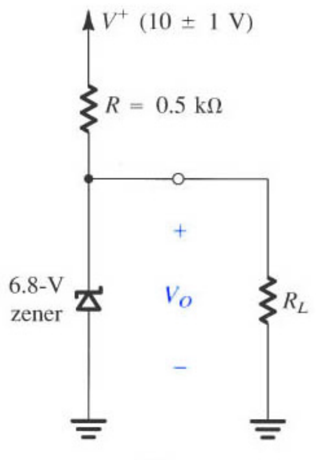
$$r_Z = \text{Constant}$$

$-V_{ZK}$ can be “tailored” during manufacture and an extensive array of Zener diodes with different $-V_{ZK}$ values (Q points) are commercially available.



e.g., A Zener diode "voltage regulator":

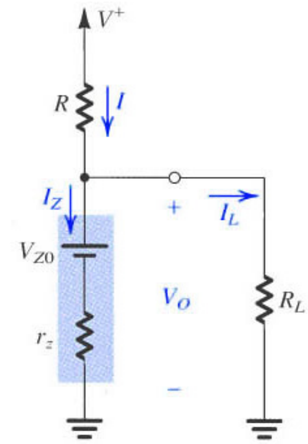
Consider the following circuit where the Zener diode is characterized by $V_{ZK}=6.69\,\text{V}$, $I_{ZK}=0.2\,\text{mA}$, $r_Z=20\,\Omega$ and $V_Z=6.8\,\text{V}$ @ $I_Z=5$ mA. Determine (*a*) V_O when $R_L=\infty$ (no load), (*b*) $R_{L(min)}$ (the maximum load), (*c*) the *Line Regulation* and *Load Regulation*.



equivalent circuit
provided Z is in
BKD*!*

calculate from specs →

$V_{Z0}=6.8\,\text{V}-(20\Omega)(5\text{mA})$
$=6.7\,\text{V}$



(*a*) When $R_L=\infty$, $I_L=0$ $\Rightarrow$ $I=I_Z=\dfrac{V-V_{Z0}}{R+r_Z}=\dfrac{10\ V-6.7\ V}{500\ \Omega+20\ \Omega}=6.35\text{ mA}$

$$\therefore\ V_O=V_Z=V_{Z0}+r_ZI_Z=6.7\text{ V}+(20\ \Omega)(6.35\text{ mA})=6.83\text{ V}$$

Alternatively, using the Superposition Principle, V_O under arbitrary load conditions is given by

$$V_O=V_{Z0}\frac{R\|R_L}{r_Z+R\|R_L}+V\frac{r_Z\|R_L}{R+r_Z\|R_L}$$

and hence when $R_L=\infty$, this expression simplifies to

$$V_O=V_{Z0}\frac{R}{r_Z+R}+V\frac{r_Z}{R+r_Z}=6.83\text{ V}$$

(*b*) The Zener must remain in BKD, which requires that $I_Z \geq I_{ZK}$ under all load conditions. The maximum load $R_L=R_{L(min)}$, therefore occurs when $I_Z=I_{ZK}$ & $V_Z=V_{ZK}$, and when the supply voltage $V=9$ V.

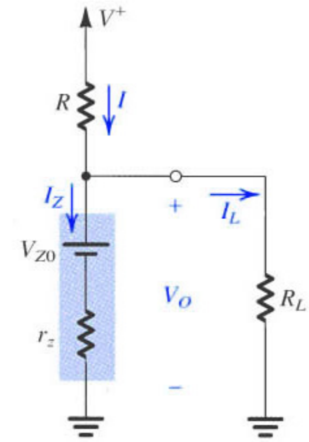
$$I_L=I-I_{ZK}=\frac{V-V_{ZK}}{R}-I_{ZK}=\frac{9\text{ V}-6.69\text{ V}}{500\ \Omega}-0.2\text{ mA}=4.42\text{ mA}$$

$$\therefore\ R_{L(min)}=\frac{V_{ZK}}{I_L}=\frac{6.69\text{ V}}{4.42\text{ mA}}=1.51\,\text{k}\Omega$$

(*c*) The *Line Regulation* & *Load Regulation* are figures of merit that characterize the performance of the voltage regulator.

$$\textit{Line Regulation}\equiv\left.\frac{\Delta V_O}{\Delta V}\right|_{I_L=\text{constant}},\quad \textit{Load Regulation}\equiv\left.\frac{\Delta V_O}{\Delta I_L}\right|_{V=\text{constant}}$$

In order to compute these figures of merit quantitatively, it is useful to write an expression for V_O that includes I_L explicitly.



Applying KCL at the node,

$$I = I_L + I_Z$$

or

$$\frac{V - V_O}{R} = I_L + \frac{V_O - V_{Z0}}{r_Z}$$

or

$$V_O = V_{Z0}\frac{R}{R + r_Z} + V\frac{r_Z}{R + r_Z} - I_L(r_Z \| R)$$

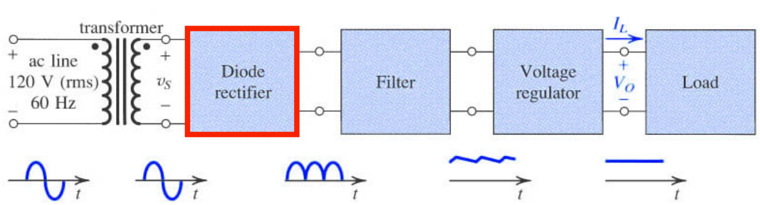
Thus, for the configuration considered here,

$$\textit{Line Regulation} \equiv \left.\frac{\Delta V_O}{\Delta V}\right|_{I_L = \text{constant}} = \frac{r_Z}{R + r_Z} = \frac{20\ \Omega}{500\ \Omega + 20\ \Omega} = 38.5\ \text{mV/V} \quad \textit{or} \quad 0.563\ \%$$

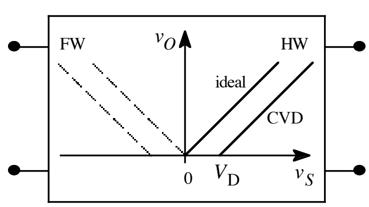
$$\textit{Load Regulation} \equiv \left.\frac{\Delta V_O}{\Delta I_L}\right|_{V = \text{constant}} = -(r_Z \| R) = \frac{(20\ \Omega)(500\ \Omega)}{(20\ \Omega) + (500\ \Omega)} = -19.23\ \text{V/A}$$

Note that the Load Regulation is independent of R_L.

Recall: DC power supply network

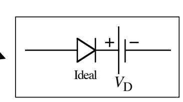


Require a circuit that “rectifies” (*i.e.*, converts) an AC (bipolar) waveform to a rectified, monopolar waveform.

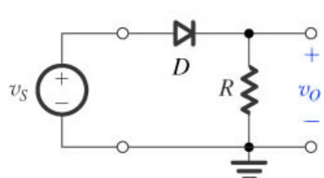


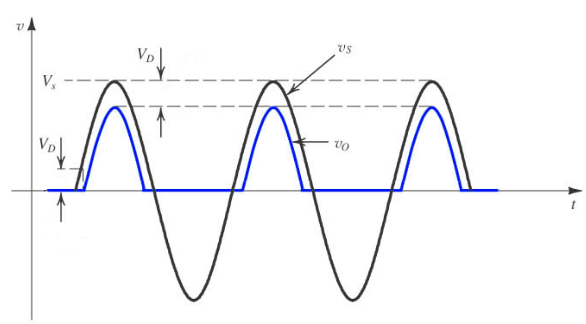
Rectifier Transfer Functions

Rectifier diodes used in power supply applications are typically modeled using either ideal diodes or a constant-voltage-drop (CVD) model.



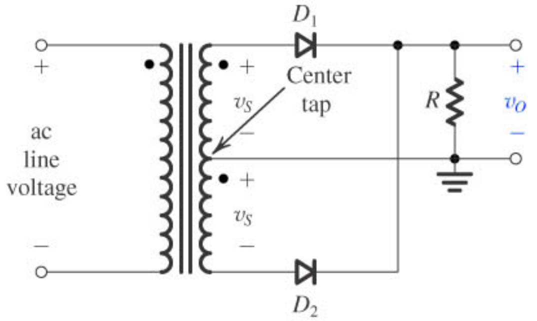
Simple Half-Wave Rectifier:

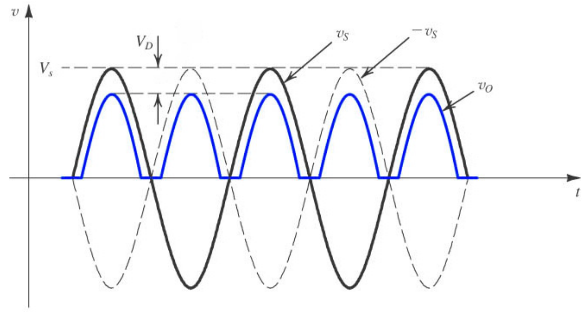




Simple Full-Wave Rectifier:

(a) *Using a Center-Tapped Transformer + 2 (Real) Diodes*





V across $D_1 > 0$ when *V* across $D_2 < 0$ and *V* across $D_1 < 0$ when *V* across $D_2 > 0$, both D_1 & D_2 conduct current through R in the same direction (when forward biased).

Peak Inverse Voltage:

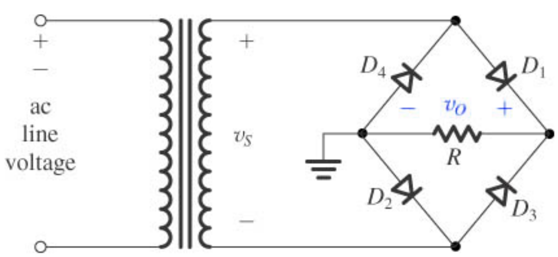
$PIV = 2V_S - V_D$ (if CVD model)

$PIV = 2V_S$ (if diodes ideal)

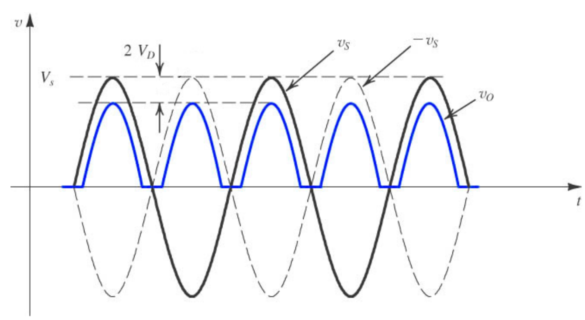
<u>Advantage</u>:
• simple—only 2 diodes required

<u>Disadvantage:</u>
• each half of the secondary is connected to the load only half of the time

(b) *Using a Simple Transformer + 4 (Real) Diodes*



Diode “Bridge” Configuration



V across D_1 & $D_2 > 0$ when *V* across D_3 & $D_4 < 0$ and *V* across D_3 & $D_4 > 0$ when *V* across D_1 & $D_2 < 0$, current through *R* is always in same direction.

Peak Inverse Voltage:

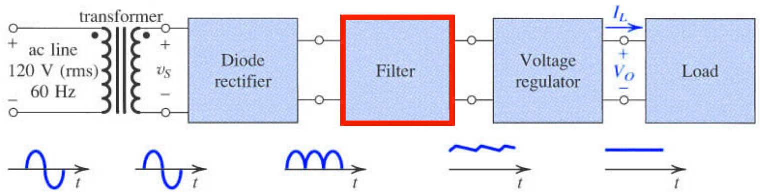
$PIV = V_S - V_D$ (if CVD model)

$PIV = V_S$ (if diodes ideal)

<u>Advantages</u>:
• no center-tap is required and fewer turns are required on the secondary winding
• the PIV is lower than 2-Diode configuration
• more efficient (the transformer secondary winding is always connected to the load)

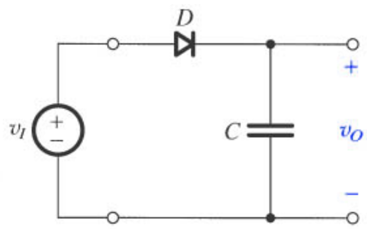
<u>Disadvantages</u>:
• common ground can not exist between the transformer secondary winding and load, *R*

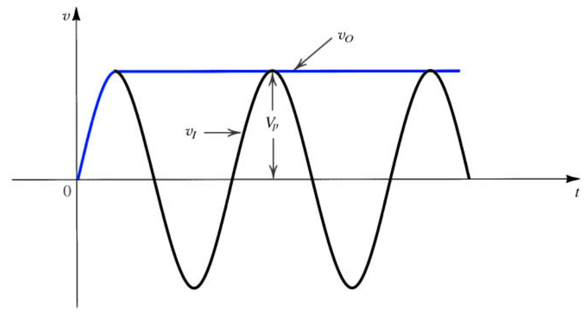
Recall: DC power supply network



Require a circuit that "smoothes" the output waveforms from the rectifier circuit.

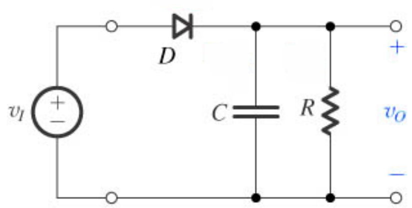
Consider the following HW rectifier circuit where the load resistance has been replaced by a capacitor:

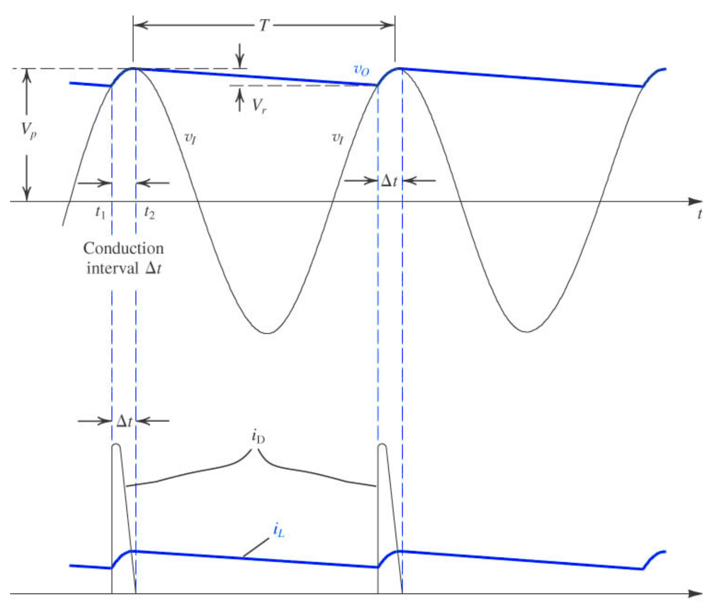




If the diode and capacitor can both be considered to be ideal, then the capacitor charges to V_p and the output voltage *remains* clamped at V_p. This circuit can be viewed as a "peak detector" (with an infinite load resistance).

In practical circuits, some finite load resistance always exists (*e.g.*, the input impedance of subsequent stages), through which C can discharge during the diode "off cycle".





This circuit is, essentially, a low-pass filter which attenuates the harmonics left in the rectified AC waveform on the cathode side of the diode.

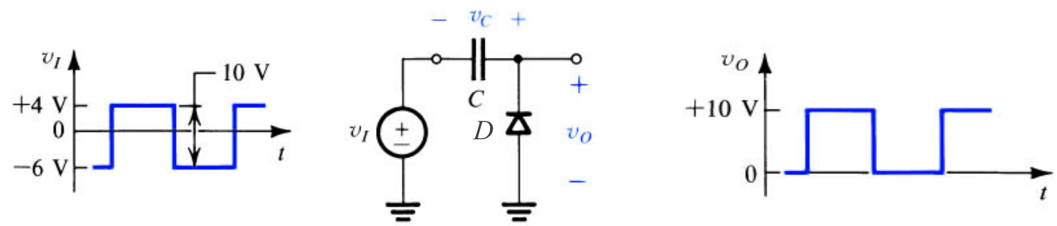
A piecewise approximate analysis of this prototypical peak rectifier yields several equations useful for the design/analysis of DC power supply circuits (see separate set of notes on WWW site).

Diode Applications: Waveshaping Circuits

Consider the following alternative diode-capacitor configurations:

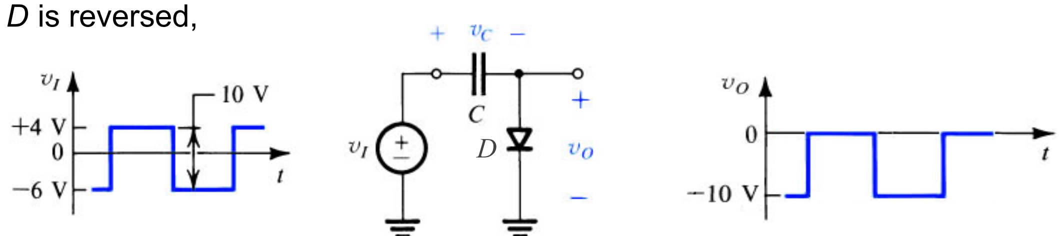
e.g., Clamped-Capacitor DC Restorer (another bipolar-to-monopolar converter).

(a) If all components are ideal,

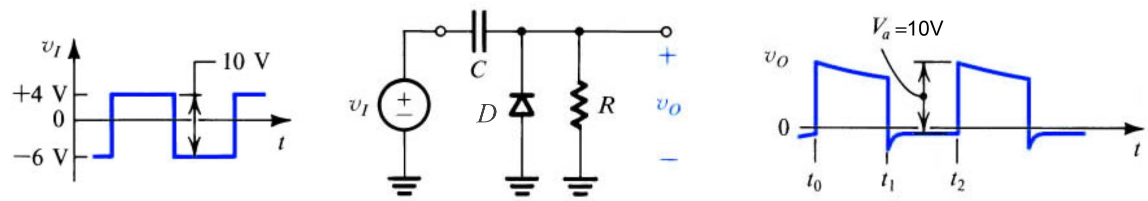


Here, D is forward biased only when $v_i < v_c$. Hence, C charges to the most negative peak of v_i (during the first few cycles) and D remains reverse biased thereafter.

If D is reversed,



(b) If $R < \infty$ and, V_{D0} & $r_D > 0$, but the capacitor is still ideal,



Assume V_{D0} = 0.7 V, and a steady state output waveform has been reached.

During the positive part of the input waveform (when D is reverse biased), C discharges through R such that

$$v_O(t) = 4\text{V} + \left[-4\text{V} - (-4\text{V} - 5.3\text{V})e^{-(t-t_0)/\tau_1}\right]$$
$$= (9.3\text{V})e^{-(t-t_0)/\tau_1}\ ; \quad t_0 \le t \le t_1$$

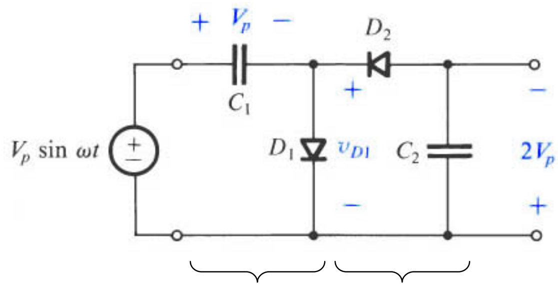
where $\tau_1 = RC$. During the negative part of the input waveform, C recharges through r_D such that

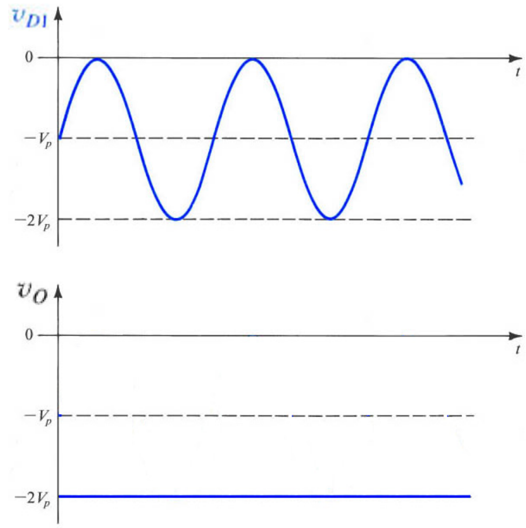
$$v_O(t) = -6\text{V} + \left[5.3V - (5.3V - 9.3e^{-(t_1-t_0)/\tau_1} + 4\text{V})e^{-(t-t_1)/\tau_2}\right]$$
$$= -0.7\text{V} - (9.3\text{V} - 9.3e^{-(t_1-t_0)/\tau_1})e^{-(t-t_1)/\tau_2}\ ; \quad t_1 \le t \le t_2$$

where $\tau_2 = (r_D || R)C$. Normally, one would try to arrange that $r_D << R$.

e.g., Voltage Doubler.

Consider a “clamped-capacitor” cascaded with a “rectifier/peak detector” as shown:





Here, the clamping circuit comprised of C_1 and D_1 determines v_{D1}, which becomes the input to the peak rectifier/detector comprised of C_2 and D_2.

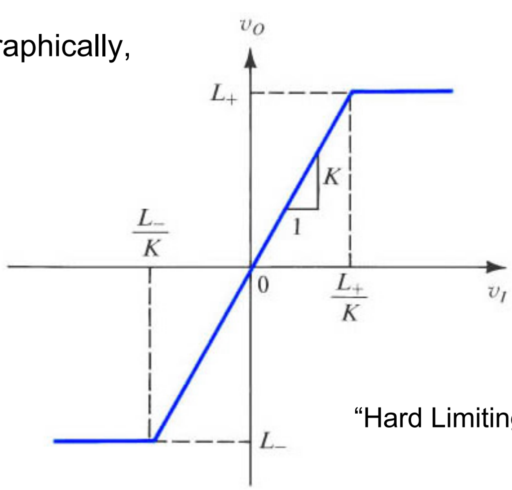
If C_1 and D_1 are ideal, then C_1 will charge to V_p, which provides a dc offset of $-V_p$ to the signal passed to the peak rectifier and C_2 will charge to $-2V_p$ (*i.e.*, the negative "peak" voltage passed from the clamp). And if C_2 and D_2 are ideal, then $V_O = -2V_p$ = constant.

Limiting or Clipping Circuits:

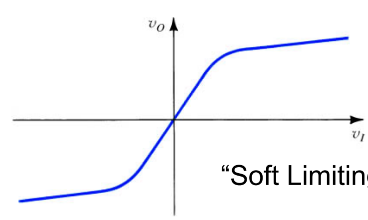
The general transfer characteristic of a limiter circuit is described by

$$
\begin{aligned}
v_o &= K\, v_i\,; && L_-/K \le v_i \le L_+/K \quad (\textit{i.e.}, \text{ linear})\\
&= L_+\,; && v_i > L_+/K\\
&= L_-\,; && v_i < L_-/K
\end{aligned}
$$

or, graphically,



“Hard Limiting”



“Soft Limiting”

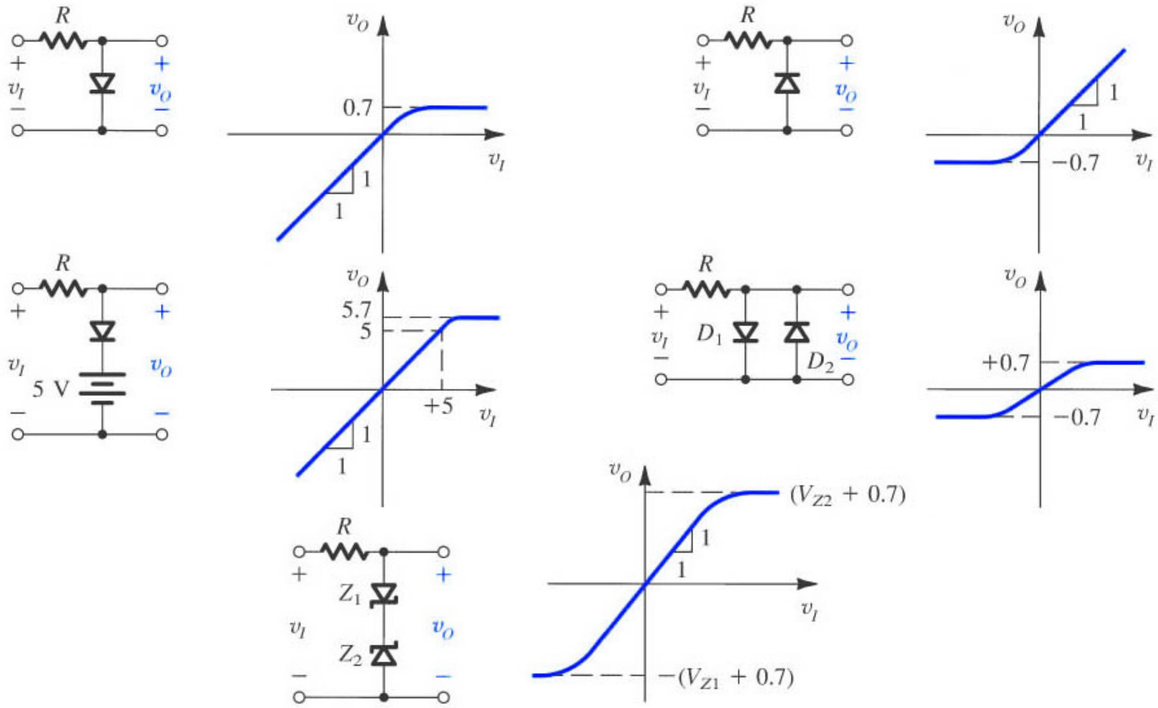
Passive Limiter: 0 < |K| < 1

Active Limiter: 0 < |K|

Limiting circuits can be realized using regular or Zener diodes and resistors in various configurations.

e.g., Various diode limiter circuits.

Consider each of the following circuits where the diodes can be assumed to be adequately modeled using a constant-voltage-drop model with V_D = 0.7 V:



Other Types of Diodes

We have considered some of the common diode types (signal, rectifier, Zener) and applications (logic circuits, AC rectification, voltage regulation, waveshaping). However, there are numerous other specialized diode types that have been modified/adapted for other applications. For example...

Photodiodes:

Semiconductor devices are subject to optical charge carrier generation leading to generation of (usually) spurious or unwanted “photocurrents” when the diode is reverse biased. Therefore, most diodes are packaged in light blocking materials. However, some applications (*e.g.*, solar cells, photodetectors) actually exploit these effects and diodes designed for such applications are packaged in transparent materials.

Light-Emitting Diodes (LEDs):

Conversely, some diodes actually emit light when forward biased, and this can be exploited for generating signals or optically-encoded information. Depending on material, colors from the infrared to the near ultraviolet may be produced; “white” LEDs are actually combinations of three LEDs of a different color, or employ coatings that filter the spectrum. An LED may be paired with a photodiode or phototransistor in the same package, to form an opto-isolator.

Schottky-Barrier Diodes:

These devices differ from other diodes in that their rectifying junction is formed by a special metal-semiconductor junction, instead of a standard *pn*-junction. Their forward voltage drop is typically in the range 0.15 V to 0.45 V, which makes them useful in voltage clamping applications; they can also be used as low-loss rectifiers, although their reverse leakage current is generally higher than *pn*-junction diodes. They also tend to have much lower capacitance than *pn*-junction diodes enabling fast switching speeds which are exploited in high-speed circuits and RF devices.

Esaki or Tunnel Diodes:

These diodes have a region in their iv-characteristic exhibiting negative resistance caused by quantum tunneling, allowing amplification of signals and very simple bistable circuits. These diodes are also the type most resistant to nuclear radiation.

Varactors:

These diodes exploit the voltage-dependent capacitances that are among the intrinsic properties of *pn*-junctions.

Etc.

In order to appreciate the full potential of these "simplest" semiconductor devices, we must first understand their structure and physical operation...