



EECE256 Assignment 6

1. Design a four bit binary synchronous counter with D flip-flops and logic gates.

4 bit binary counter counter

present	next
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	0000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

CD

AB	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	1	1	0	1
10	1	1	1	1

$D_A = AB' + A(C'+D') + A'BCD$

CD

AB	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	0	0	0	1
10	0	0	0	1

$D_B = B(C'+D') + B'(CD)$

CD

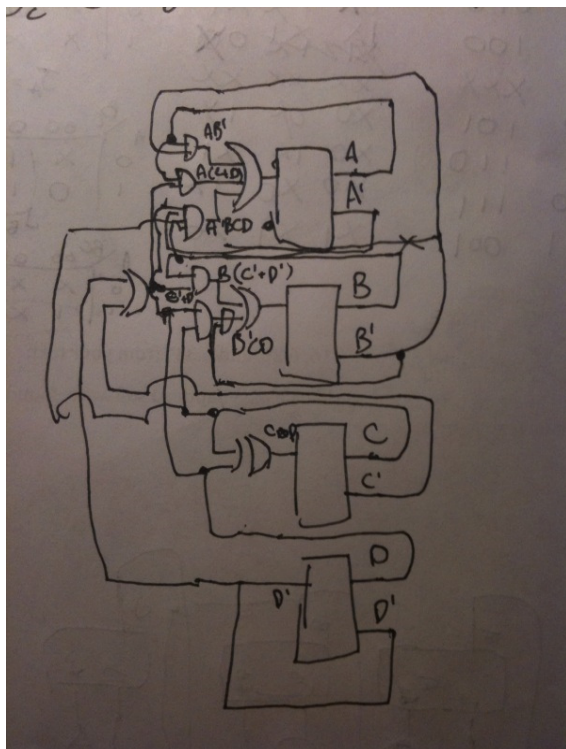
AB	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

$D_C = C \otimes D$

CD

AB	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	1	0	0	1
10	1	0	0	1

$D_D = D'$





a place of mind

2. Design a counter which cycles through the binary sequence (1,2,4,5,6,7) using J/K flip-flops. Show that when states 000 and 011 are used as don't care statements the counter may not operate properly. Suggest how to correct this problem.

may not operate properly. Suggest how to co

		J_A	K_A	J_B	K_B	J_C	K_C
000	xxx	xx	x	xx	x	xx	x
001	010	0	1	x	x	1	1
010	100	1	x	x	0	0	x
011	xxx	xx	xx	xx	xx	xx	xx
100	101	x	0	0	x	1	x
101	110	x	0	1	x	x	1
110	111	x	0	x	0	1	x
111	001	x	1	x	1	x	0

rect this problem.

A	BC	00	01	11	10
0		x	0	x	1
1		x	x	x	x

$J_A = B$

A	BC	00	01	11	10
0		x	x	x	x
1		0	0	1	0

$K_A = BC$

A	BC	00	01	11	10
0		x	1	x	x
1		0	1	x	x

$J_B = C$

A	BC	00	01	11	10
0		x	x	x	1
1		x	x	1	0

$K_B = C + A$

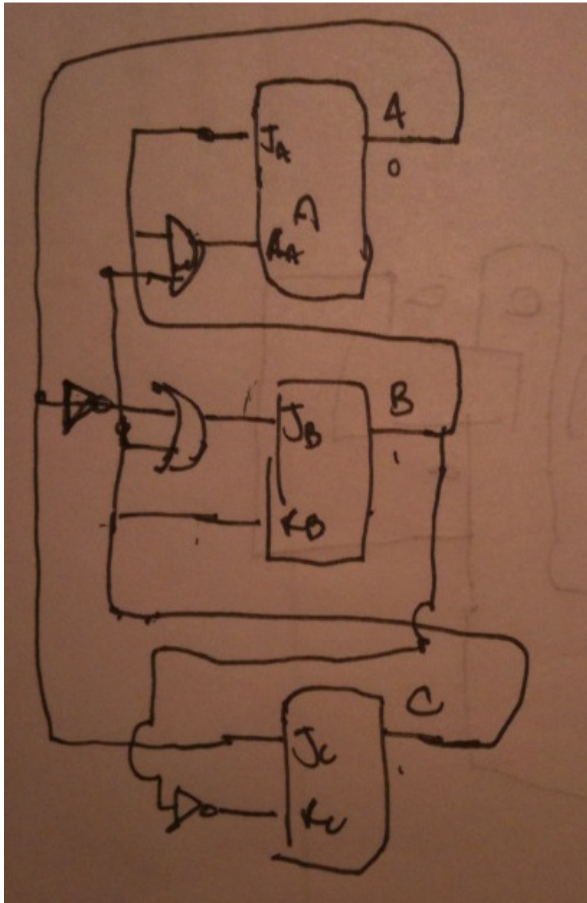
A	BC	00	01	11	10
0		x	x	x	0
1		1	x	x	1

from your text. $J_C = A$

A	B	00	01	11	10
0		x	1	x	x
1		x	1	0	x

$K_C = B'$

software, found on the CD included with



State transition during unknown state values

000 → 011

011 → 101

Force unknown states to state 001 or create an error state output

in the CD included with