1. **[30 points]** Short Questions

1.a. Prove or disprove that the operators ($\Rightarrow$,XOR) form a complete set. Remember that the operator ($\Rightarrow$) is implication such that:

A	B	$A \Rightarrow B$
0	0	1
0	1	1
1	0	0
1	1	1

1.b. Realize a 5-input NOR function using 2-input NOR gates only.

1.c. Implement the function $F(A,B,C) = \Sigma m(1,2,4,5,7)$ using a 4:1 multiplexer (you also have GND and +5V available).

1.d. Implement both the two-input NAND and two-input NOR functions together using a single 2-to-4 decoder and a minimal number of additional OR gates.

1.e. Given that AB = 0 and A + B = 1, prove:

AC + A'B + BC = B + C

1.f. Implement the following three functions using a PLA with two AND gates and 3 OR gates (show the PLA logic)

F(A,B,C) = ABC' + ABC
G(A,B,C) = A'BC + A'C
H(A,B,C) = A'B'C + BC + ABC'

2. **[20 points]** A reset-dominate latch has a **set** (L) and a **reset** (M) input. It differs from a conventional RS latch in that an attempt to simultaneously set and reset the latch (i.e., when L=1 and M=1) results in **setting** the latch so that it stores a 1. In a normal RS latch these would be forbidden inputs.

2.a. Derive the excitation table for this latch. **REMEMBER: L = set and M = reset!**
2.b. Derive the characteristic equation for this latch.
2.c. Show a logic diagram of this LM latch using only NOR gates and one 2-input AND gate if needed.

3. **[30 points]** Short Questions

3.a. Demonstrate de Morgan's theorem for **three** variables using a truth table.

3.b. Realize a 5-input NAND function using 2-input NAND gates only.

3.c. Implement the function $F(A,B,C) = \Sigma m(0,3,6)$ using a 4:1 multiplexer.

3.d. Implement the two-input NAND and two-input NOR functions using a single 2-to-4 decoder and a minimal number of additional OR gates.

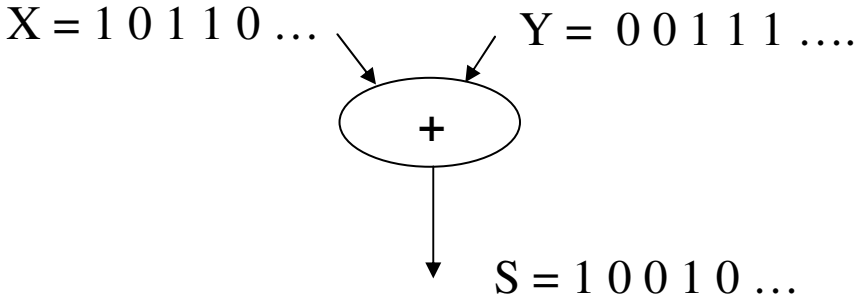
3.e. Using theorems of Boolean algebra, prove the following :

$$BD'E + ABCE + CDE = BD'E + CDE$$

3.f. Implement the following three functions using a PLA with two AND gates and 3 OR gates (show the PLA logic)

$F(A,B,C) = ABC' + ABC$
$G(A,B,C) = A'BC + A'C$
$H(A,B,C) = A'B'C + BC + ABC'$

4. **[15 points]** A serial adder is a circuit that has two inputs (X and Y) and one output (S). The inputs represent two binary numbers that have bit values that appear serially beginning with the lowest significant bit first. The output is the serial sum of the two numbers. The diagram below shows the behavior of this circuit for two numbers, X = …01101 and Y = …11100 and the sum is S = …01001. Draw a state diagram for the serial adder.



5. **[30 points]** Below is a state diagram showing a counter with a single input, X. When X is high the counter counts odd number and when it is low it counts even numbers.

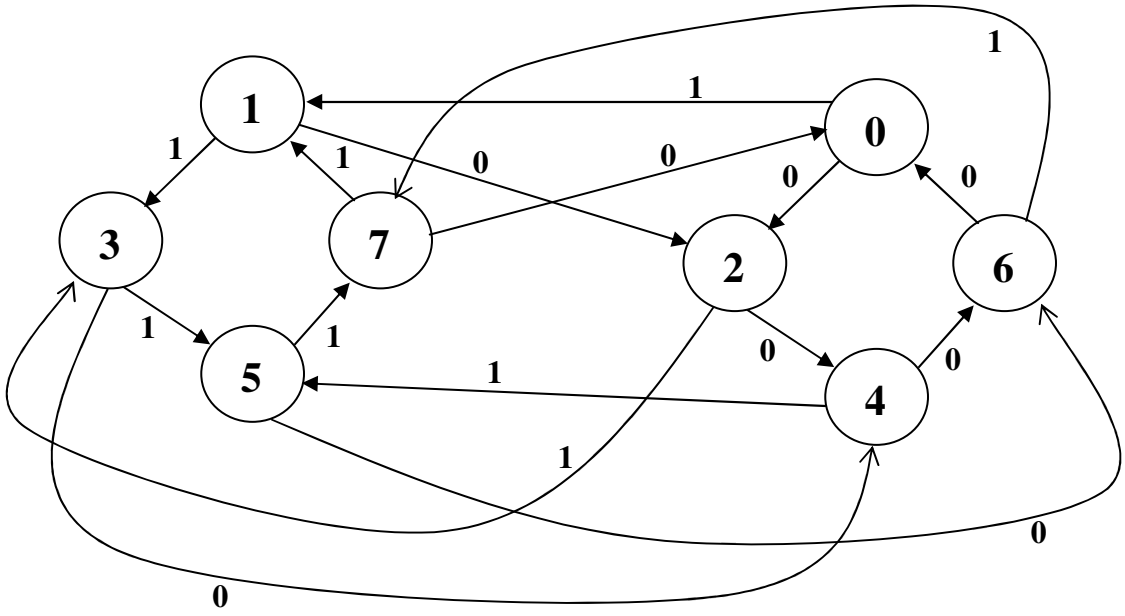
5.a. Draw the state transition table for this state diagram including:

5.a.1. the next state,

5.a.2. the remapped state transitions for a T flip-flop implementation and

5.a.3. the remapped state transitions for a JK flip-flop implementation.

5.b. Implement and draw the circuit using only three 8-to-1 multiplexers and T flip-flops.



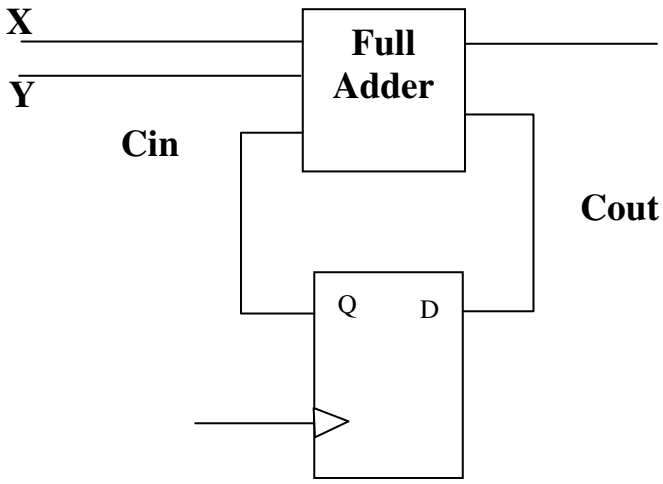
State Diagram of an odd/even counter.

6. **[15 points]** For the state machine below:

6.a. Is it a Moore machine or a Mealy machine?

6.b. Show the state table for the circuit.

6.c. Show the state diagram for the circuit.

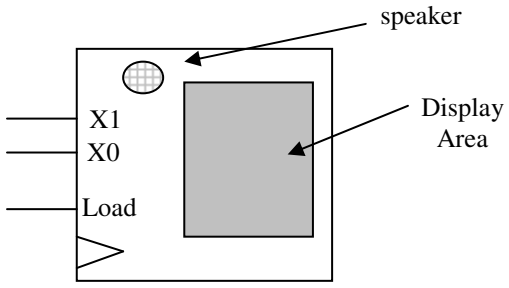


7. **[20 points]** I would like a FSM to help me assign grades for each student in my courses. The way I want the machine to work is that there are two inputs to the FSM: the first input is a start signal to start the machine and the second signal represents the toss of a coin. If the coin toss is Tails the signal is low (0) and if the coin toss is Heads the signal is high (1). The output is a mark of either 68%, 72%, 76% or 80%. First, I start the machine. To assign a grade, for each student, I start with a mark of 68%. Each student has up to four coin tosses to determine their mark. The number of **Heads, in a row**, determines how high their mark goes. As soon as a Tails appears their mark is displayed in a special display described below, and the system will be ready for the next student. The maximum mark is 80% that is assigned if three Heads are flipped in a row. After the maximum mark is achieved the next coin flip will display the mark and the system will be ready for the next student. Here are example coin tosses for some students:

T = 68%
H,T = 72%
H,H,T = 76%
H,H,H,T = 80%
H,H,H,H = 80%

You have available a special display block available to use. It has four inputs: X0, X1, Load, and the clock. The Load signal **synchronously** loads the values of X0 and X1 into the display. The display also makes a beep sound whenever the display is loaded to let me know to record the mark for the current student and move on to the next student. The special display decodes X0 and X1 according to this table:

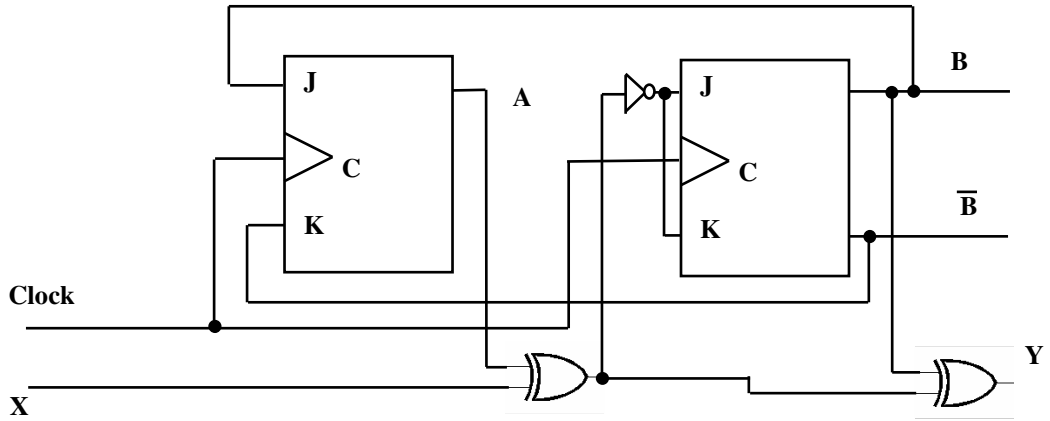
X1	X0	Display
0	0	72%
0	1	76%
1	0	80%
1	1	68%



Your task is to design a **Mealy** machine to implement the above FSM.

7.a. First, draw the state diagram for this machine.
7.b. Second, show your final design using a circuit diagram of your **Mealy** machine. Use only **JK flip-flops** that have **asynchronous** Set and Reset pins, the display block provided and any additional combinational circuitry you need. Show your steps for arriving at your final design.

8. **[20 points]** Given the following sequential circuit that uses two JK flip-flops:



8.a. Derive the next-state equations, i.e. expressions for A^+ and B^+, and the output equation.

8.b. Show the state table

8.c. Show the state diagram for the machine