a place of mind

Electrical and Computer Engineering

Nov 26, 2010

EECE256 Quiz 4 – section 101

1. Specify the parity equations for a 5 bit number, and show the parity + data representation. Include a parity bit to do single error correction, multiple error correction. (5 marks)

num: $b_0\ b_1\ b_2\ b_3\ b_4$ $\Rightarrow$ p+num : $P_1\ P_2\ b_0\ P_4\ b_1\ b_2\ b_3\ P_8\ b_4\ P_{10}$ (positions 1 2 3 4 5 6 7 8 9 10)

(1) $P_1 = XOR(b_0, b_1, b_3, b_4)$ (3, 5, 7, 9)

(1) $P_2 = XOR(b_0, b_2, b_3)$ (3, 6, 7)

(1) $P_4 = XOR(b_1, b_2, b_3)$ (5, 6, 7)

(1) $P_8 = XOR(b_4) = b_4$ (9)

(1) $P_{10} = XOR(P_1, P_2, \ldots b_4) =$ even parity

What is the parity + data of the numbers: (1)

01110? (1 mark) $P_1 = XOR(0,1,1,0) = 0$, $P_2 = XOR(0,1,1) = 0$, $P_4 = XOR(1,1,1) = 1$, $P_8 = 0$, $P_{10} = 0$ $\Rightarrow$ 00011110000

10101? (1 mark) $P_1 = XOR(1,0,0,1) = 0$, $P_2 = XOR(1,1,0) = 0$, $P_4 = XOR(0,1,0) = 1$, $P_8 = XOR(b_4) = 1$, $P_{10} = 1$ $\Rightarrow$ 00110101111 (1)

2. What are the three stages of computer aided design (CAD) that are used to compile a verilog circuit onto an FPGA? (3 marks)

- Synthesis (1)
- Placement (1)
- Routing (1)

3. Draw the truth table for a programmable array logic (PAL) with 3 input OR gates, and a single feedback term which implements the following functions:

X = AB'C + ACD+A'B'

Y = AC + AB'D+AB'

Z = AB + AC'D' + B'CD + C'D

(4 marks)

if $w = AB + AC'D'$ $\Rightarrow$

A	B	C	D	w	
-	-	-	-	1	
-	0	1	1	-	Z
-	-	0	1	-	

A	B	C	D	
1	0	1	-	
1	-	1	-	X
0	0	-	-	
1	-	1	-	
1	0	-	1	Y
1	0	-	-	
1	-	0	0	
-	0	1	1	Z
-	-	0	1	
1	1	-	-	
1	1	-	-	
1	-	0	0	W

Specify the connections which will program the PAL shown below to implement your circuit. Be sure to specify what the AND gate inputs to the PAL are. (3 marks)