



# EECE256 Quiz 4 – section 101

1. Specify the parity equations for a 5 bit number, and show the parity + data representation. Include a parity bit to do single error correction, multiple error detection. (5 marks)

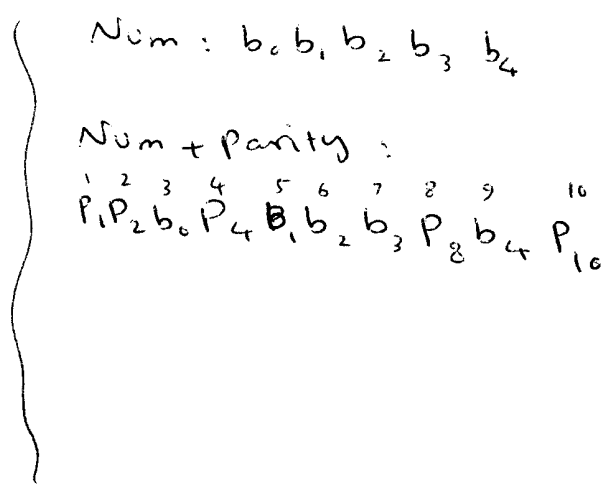
$$P_1 = \text{XOR}(3, 5, 7, 9)$$

$$P_2 = \text{XOR}(3, 6, 7)$$

$$P_4 = \text{XOR}(5, 6, 7)$$

$$P_8 = \text{XOR}(9)$$

$$P_{16} = \text{XOR}(P_1, P_2, \dots, b_4)$$



What is the parity + data of the numbers:

10011? (1 mark)

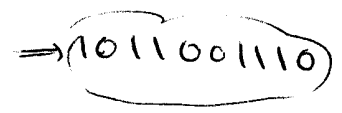
$$P_1 = \text{XOR}(1, 0, 1, 1) = 1$$

$$P_2 = \text{XOR}(1, 0, 1) = 0$$

$$P_4 = \text{XOR}(0, 0, 1) = 1$$

$$P_8 = 1$$

$$P_{16} = 0$$



01101? (1 mark)

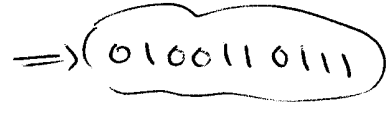
$$P_1 = \text{XOR}(0, 1, 0, 1) = 0$$

$$P_2 = \text{XOR}(0, 1, 0, 1) = 1$$

$$P_4 = \text{XOR}(1, 1, 0) = 0$$

$$P_8 = 1$$

$$P_{16} = 1$$



2. What are the three major block types of an FPGA? (3 marks)

- Switch Matrix
- CLB (Configurable Logic Block)
- I/O Block (IOB)



# a place of mind

Electrical and Computer Engineering

Nov 23, 2010

3. Draw the truth table for a programmable array logic (PAL) with 3 input OR gates, and a single feedback term which implements the following functions:

$$X = ABC' + A'CD + AB'$$

$$Y = A'C + A'D + A'B'$$

$$Z = A'B + A'BC' + A'CD' + B'D$$

(5 marks)

① First Solution:  $A'B + A'BC' = A'B(1 + C') = A'B$

$\Rightarrow Z = A'B + A'CD' + B'D \Rightarrow$  No feedback is required

② Second Solution:

$A'B + A'BC' = W \Rightarrow$

A	B	C	D	W	Z
-	-	-	-	1	
0	-	1	0	-	
-	0	-	1	-	

For the other outputs:

A	B	C	D	X	Y	W
1	1	0	-			
0	-	1	1			
1	0	-	-			
0	-	1	-			
0	-	-	1			
0	0	-	-			
0	1	-	-			
0	1	0	-			



# a place of mind

Specify the connections which will program the PAL shown below to implement your circuit. Be sure to specify what the AND gate inputs to the PAL are. (3 marks)

