a place of mind
Electrical and Computer Engineering

Nov 23, 2010

EECE256 Quiz 4 – section 101

1. Specify the parity equations for a 5 bit number, and show the parity + data representation. Include a parity bit to do single error correction, multiple error detection. (5 marks)

$P_1 = XOR(3,5,7,9)$ $(0,1,3,4)$

$P_2 = XOR(3,6,7)$ $(0,2,3)$

$P_4 = XOR(5,6,7)$ $(1,2,3)$

$P_8 = XOR(9)$

$P_{16} = XOR(P_1, P_2, \ldots, b_4)$

Num : $b_0 b_1 b_2 b_3 b_4$

Num + Parity :

$P_1 P_2 b_0 P_4 b_1 b_2 b_3 P_8 b_4 P_{16}$

(1 2 3 4 5 6 7 8 9 10)

What is the parity + data of the numbers:

10011? (1 mark)

$P_1 = XOR(1,0,1,1) = 1$ $P_8 = 1$

$P_2 = XOR(1,0,1) = 0$ $P_{16} = 0$

$P_4 = XOR(0,0,1) = 1$

$\Rightarrow 1011001110$

01101? (1 mark)

$P_1 = XOR(0,1,0,1) = 0$ $P_4 = XOR(1,1,0) = 0$

$P_2 = XOR(0,1,0) = 1$ $P_8 = 1$ $P_{16} = 1$

$\Rightarrow 0100110111$

2. What are the three major block types of an FPGA? (3 marks)

- Switch Matrix
- CLB (Configurable Logic Block)
- I/O Block (IOB)

3. Draw the truth table for a programmable array logic (PAL) with 3 input OR gates, and a single feedback term which implements the following functions:

X = ABC' + A'CD+AB'

Y = A'C + A'D+A'B'

Z = A'B + A'BC' + A'CD' + B'D

(5 marks)

① First Solution: $A'B + A'BC' = A'B(1 + C') = A'B$

$\Rightarrow Z = A'B + A'CD' + B'D$ $\Rightarrow$ No feedback is required

② Second Solution:

$A'B + A'BC' = W$ $\Rightarrow$

A	B	C	D	W	
-	-	-	-	1	
0	-	1	0	-	Z
-	0	-	1	-	

for the other outputs:

A	B	C	D	
1	1	0	-	
0	-	1	1	X
1	0	-	-	
0	-	1	-	
0	-	-	1	Y
0	0	-	-	
0	1	-	-	W
0	1	0	-	

Specify the connections which will program the PAL shown below to implement your circuit. Be sure to specify what the AND gate inputs to the PAL are. (3 marks)