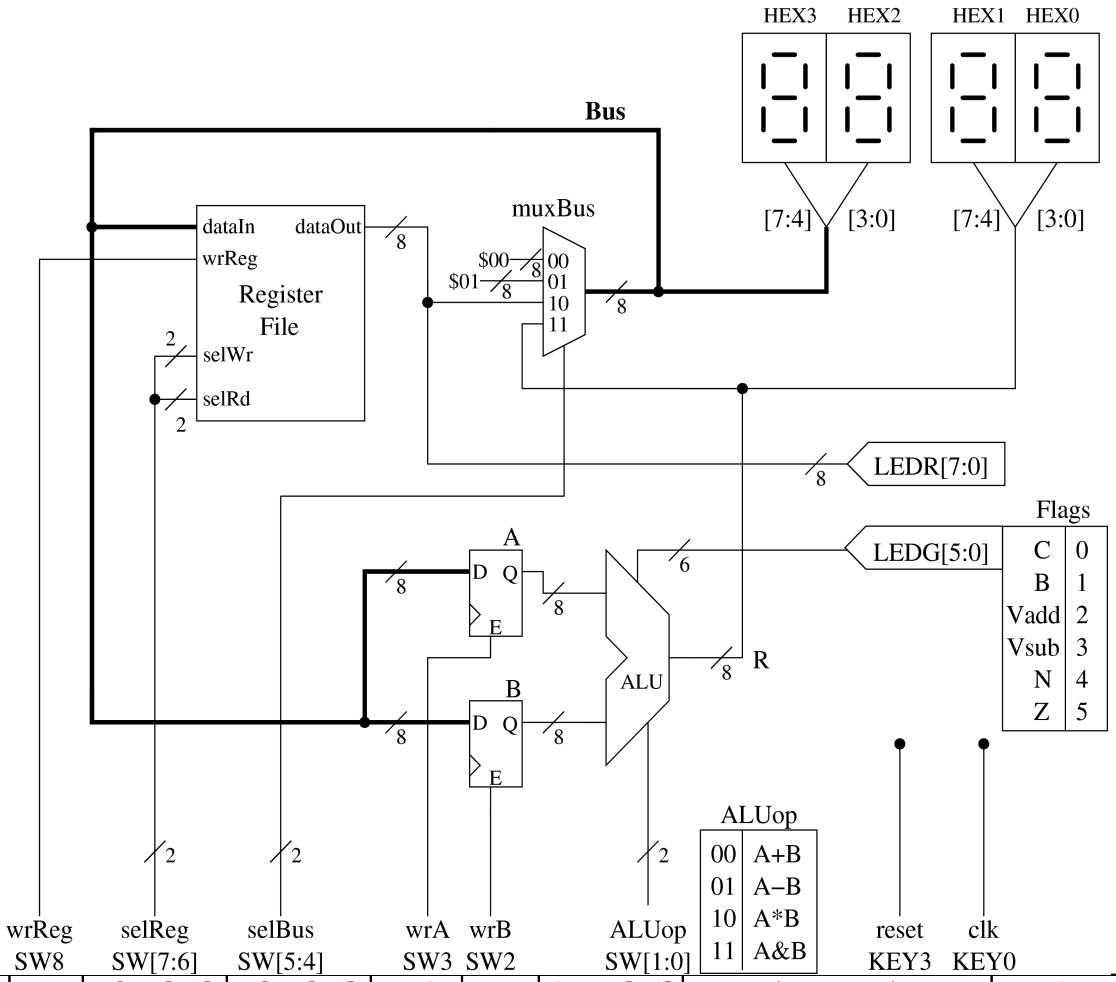

Cycle #	wrReg	selReg[1:0]	selBus[1:0]	wrA	wrB	ALUop[1:0]	Micro-operation	Overall Operation
1.								
2.								
3.								
4.								
5.								
6.								
7.								
8.								
9.								
10.								
11.								
12.								
13.								
14.								
15.								
16.								
17.								
18.								
19.								
20.								