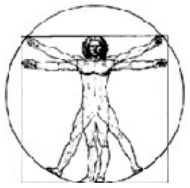
Electrical and Computer Engineering

ELEC 391
Electrical Engineering Design Studio II

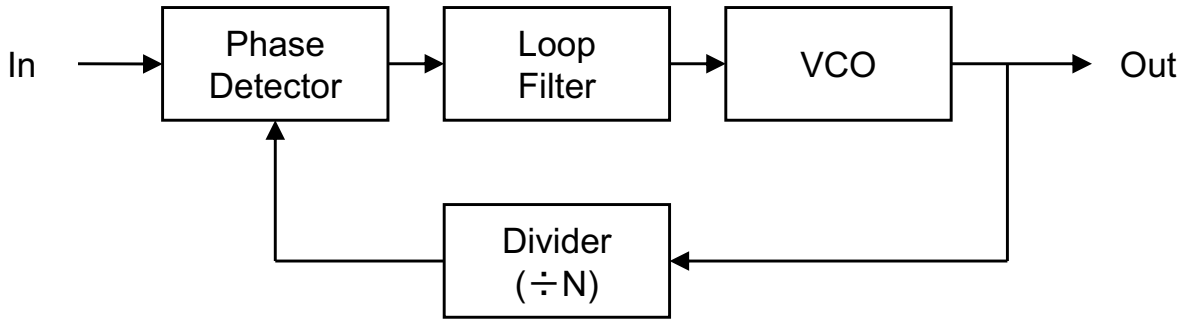


Introduction to Phase-Locked Loops

Introduction to project management. Problem definition. Design principles and practices. Implementation techniques including circuit design, software design, solid modeling, PCBs, assembling, and packaging. Testing and evaluation. Effective presentations. [2-0-4]

- During this lecture, the instructor will bring up many points and details not given on these slides. Accordingly, it is expected that the student will annotate these notes during the lecture.
- The lecture only introduces the subject matter. Students must review these notes after class and complete the reading assignments and problems if they are to master the material.

Block Diagram of a Phase-Locked Loop



A phase-locked loop is a feedback control system that is:

- based upon the *phase* of a signal rather than the *amplitude*
- an essential component of modern communications systems (and many control systems)

Introduction

- A phase-locked loop (PLL) is a feedback control system that forces the output frequency of a voltage controlled oscillator (VCO) to track the frequency of an input signal.
- In 1932, DeBellescize reported the first use of the phase-lock principle for the synchronous detection of radio signals.
- Television was the first widespread application of PLL technology, but not the last.
- During the early 1960's, NASA began using PLL's to automatically track telemetry signals when the carrier frequency drifts due to Doppler shifting or temperature effects. (Many key advances in PLL theory and design were made during this period.)
- Since the late 1960's, integrated circuit technology has made phase-locked loop technology both inexpensive and practical.

- In practice, phase-locked loops have proven to be amazingly versatile. Applications of PLL's include:
  - **frequency synthesis**
  - **FM demodulation**
  - **motor speed control**

  • to be discussed in more detail here
  - FM modulation
  - filtering
  - signal detection

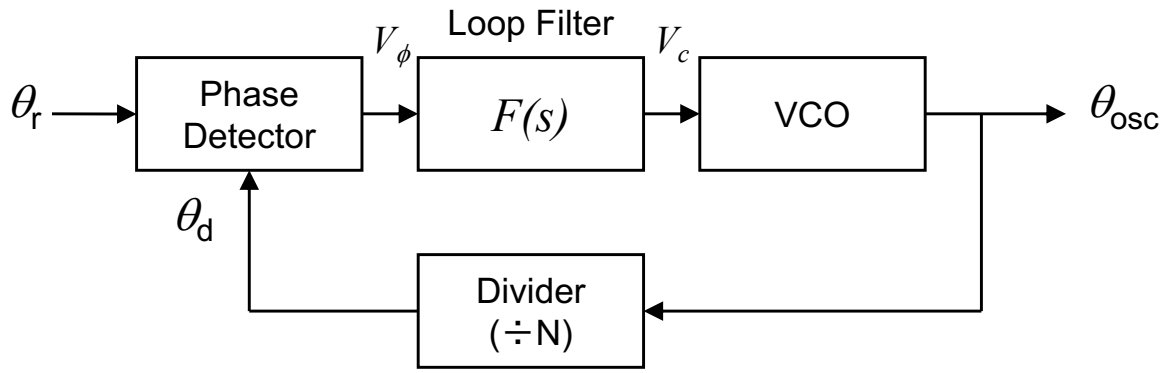
    etc.
- As a control system which has major applications in communications, phase-locked loops are an especially appropriate topic for study in ELEC 391.

Objectives

Upon completion of this briefing, you will be able to:

- Describe the basic architecture of a phase-locked loop
- Explain the function and operation of PLLs in some typical applications
- Identify the fundamental issues in phase-locked loop design
  - implementation,
  - loop filter design,
  - applications
- Describe the implementation of the classic 4046 PLL, including the phase detector, loop filter, and VCO.
- Apply these insights to other PLLs such as the LM565.

1. Basic Architecture of a Phase-Locked Loop



- The error signal V_ϕ is $V_a(t) = k(\theta_d(t) - \theta_r(t))$
- The control voltage V_c is a version of V_a that has been filtered in order to set the capture range and appropriately modify the loop dynamics.
- The VCO's output frequency is proportional to the control voltage V_c .

- The signal fed back to the phase detector has the frequency of the VCO's output signal divided by 'N'.
- The VCO control voltage changes in the direction that forces the VCO to change frequency in the direction that reduces the difference between the input and output frequencies
- If the two frequencies are sufficiently close, the loop gain will force the output from divider to precisely track the frequency of the input signal, *i.e.,*

$$f_r = f_d \, .$$

- Since $f_d = \dfrac{f_{osc}}{N}$, $\quad f_{osc} = N\, f_r$.
- For now, assume N = 1.

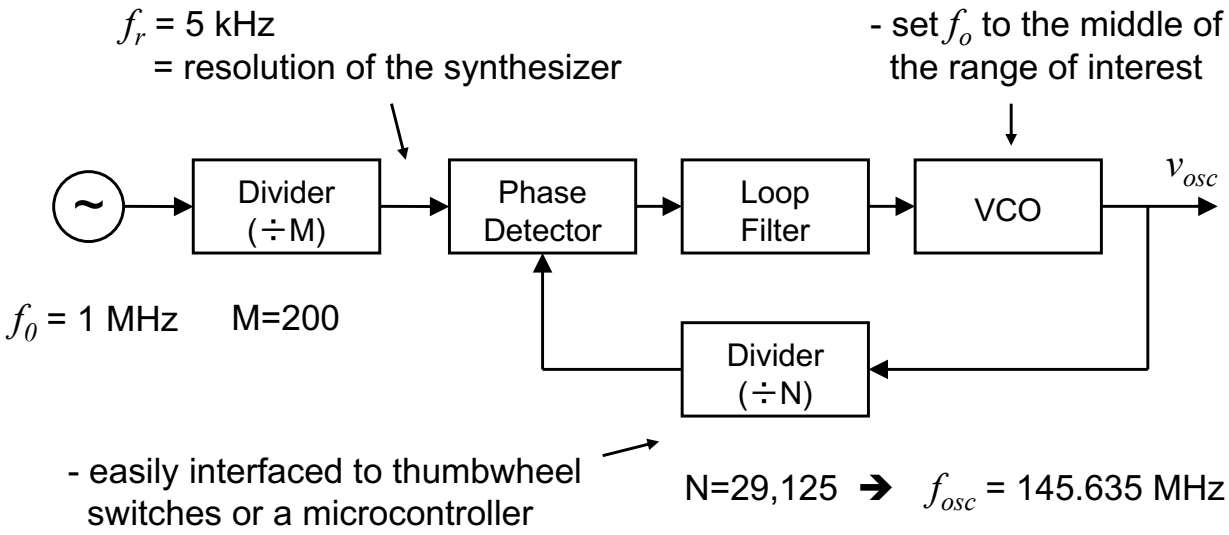
- Once the loop is in lock, there will be a small phase difference between the two phase detector input signals.
  (Why?)
- Once the PLL is locked, the frequency of the output signal will track any changes in the frequency of the input signal.
- The **capture range** is the range over which a PLL can lock onto a signal.
- The **lock range** is the range over which a PLL can track that signal.
- The lock range is always wider than the capture range!

2. Applications of Phase-Locked Loops

2.1 Frequency Synthesis

- In the "old" days, it was necessary to provide a separate crystal for every channel in a multi-channel transmitter or receiver.
- Free-running oscillators weren't – and still aren't – sufficiently stable for use in most communications applications.
- The phase-locked loop provides a means to synthesize a vast range of output frequencies using just a single crystal oscillator as a frequency reference.

A PLL-based Frequency Synthesizer

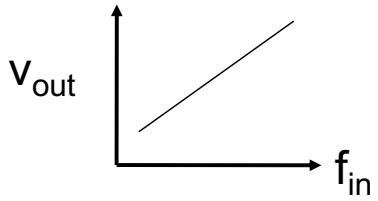


- A PLL-based synthesizer allows one to "dial up" arbitrary (but discrete) frequencies with crystal-controlled accuracy and stability

2.2 FM Demodulator

- A variety of circuits suitable for demodulating FM signals have been developed.
- Most are based upon a high pass filter with a given slope, as discussed previously.

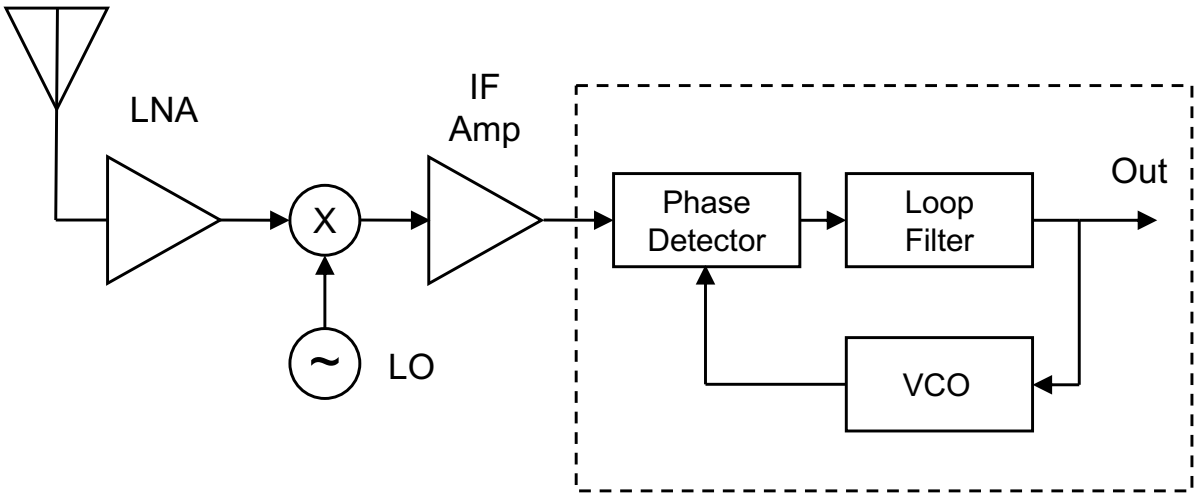
FM Demodulator Transfer Function



- However, it is fairly difficult to implement such filters using integrated circuit technology.
- Close understanding of the function and operation of phase-locked loops reveals that a Phase Locked Loop can function as an FM demodulator. How?

- Recall how a phase-locked loop functions: It forces the instantaneous output frequency of the VCO to closely track the instantaneous frequency of the input signal.
- If the input signal is FM, the output signal will also be FM, which doesn't appear to be too helpful!
- However, a VCO is, by definition, a frequency modulator.
- If the signal at the **output** of a VCO is a frequency modulated version of the original message signal, then the signal that we observe at the **input** to the VCO is a replica of the original message signal.
- By this reasoning, a phase-locked loop can be configured to function as an FM demodulator.

A PLL-based FM receiver



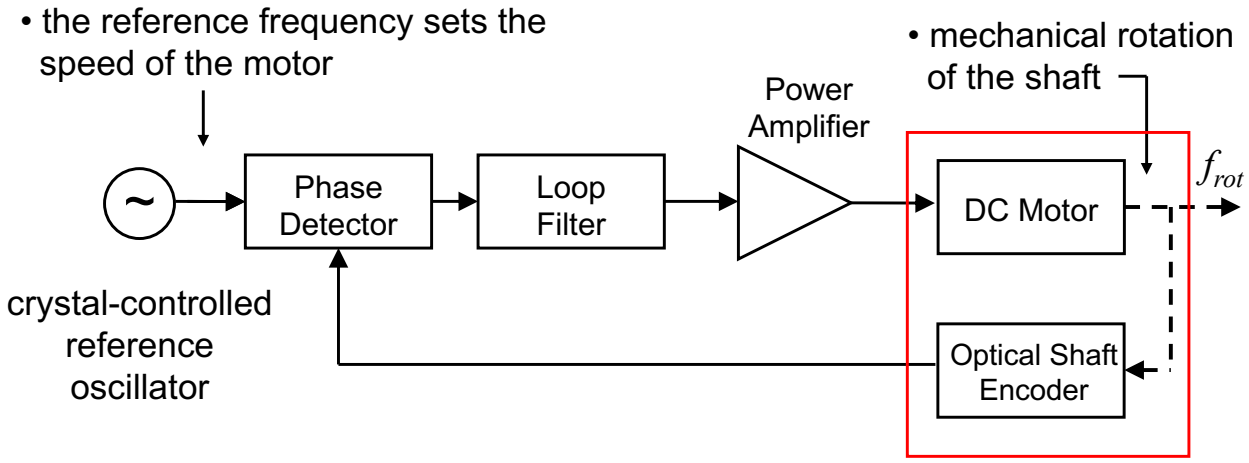
A PLL-based FM demodulator

ELEC 391 students should be able to explain the function and operation of this receiver.

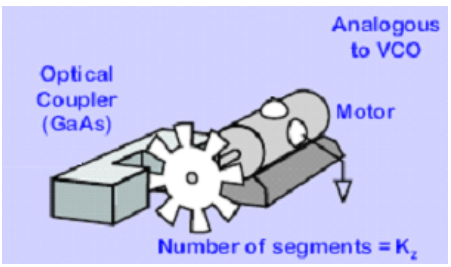
2.3 Motor Speed Control

- The PLL architecture can also be applied to precise control (or regulation) of the speed of a DC motor.
- The rotation speed of a DC motor is proportional to the applied voltage and can be sensed using an optical shaft encoder. The combination can be regarded as a mechanical VCO.
- If one compares the phase of a reference signal to the output of the shaft encoder (after division by N), one can generate an error signal that modifies the rotation speed of the motor to match N times the reference rate.
- The result allows us to set the rotation speed of the motor simply by dialing up the appropriate divide ratio.
- Is there an alternative configuration?

A PLL-based Motor Speed Controller



- A PLL-based motor speed controller allows one to "dial up" arbitrary (but discrete) rotation rates with crystal-controlled accuracy and stability. Among other places, they are used in various types of optical and magnetic disk drives,.

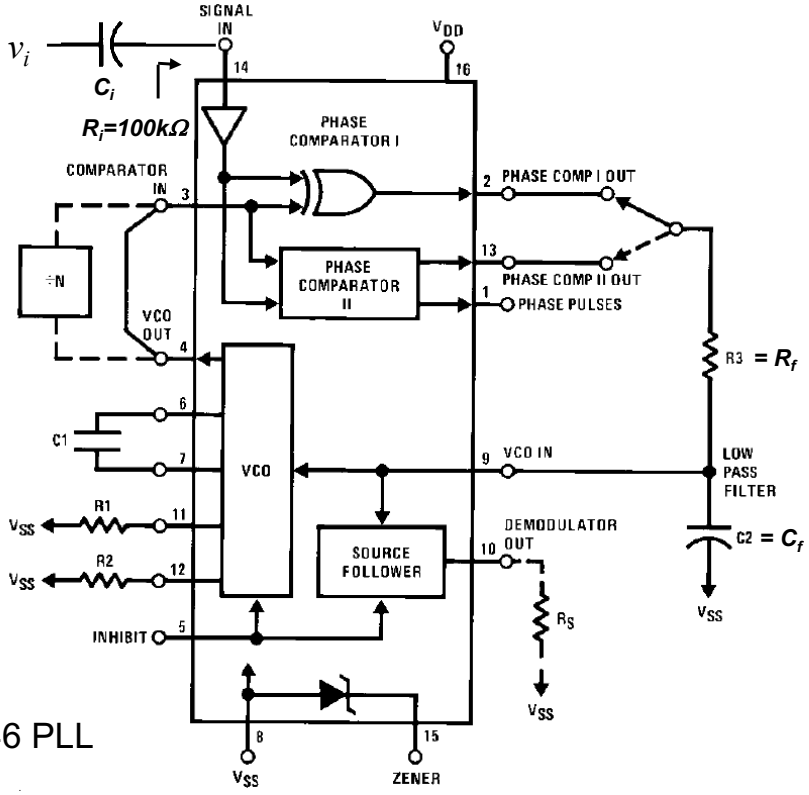


3. Issues in Phase-Locked Loop Design

- Implementation – RF Design
  - How to realize and characterize:
    - phase detectors?
    - voltage controlled oscillators?
    - high speed digital dividers?
- Loop Design (Control Systems)
  - How to design a loop filter that will yield the desired transient response (including the capture range)?
- Applications (Communications)
  - How to apply the PLL principle to new and different applications, particularly in communications?

4. Implementation of a Phase-Locked Loop

- In this final section, we focus on the 4046 PLL as an illustrative example



4046 PLL

4.1 Highlights

- 4046 Phase-Locked Loop
  - CMOS technology
  - single positive supply voltage (we'll use V_{DD} = + 15 V)

- Input Circuit
  - v_i should be ~ 1 $V_{p\text{-}p}$ for proper operation
  - R_i (~ 100 kΩ) and C_i form a high pass filter
  - select C_i so that v_i is in the pass band of the filter, *i.e.,*

$$f_i > \frac{1}{2\pi R_i C_i}$$

    for the lowest expected frequency.

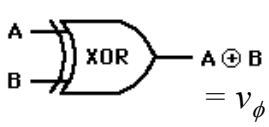
4.2 Phase Detector

- There are several ways to implement a phase detector.
- For example, one can combine an analog mixer with a low pass filter. If one applies two sinusoids with the same frequency but a phase offset, the output of the mixer is

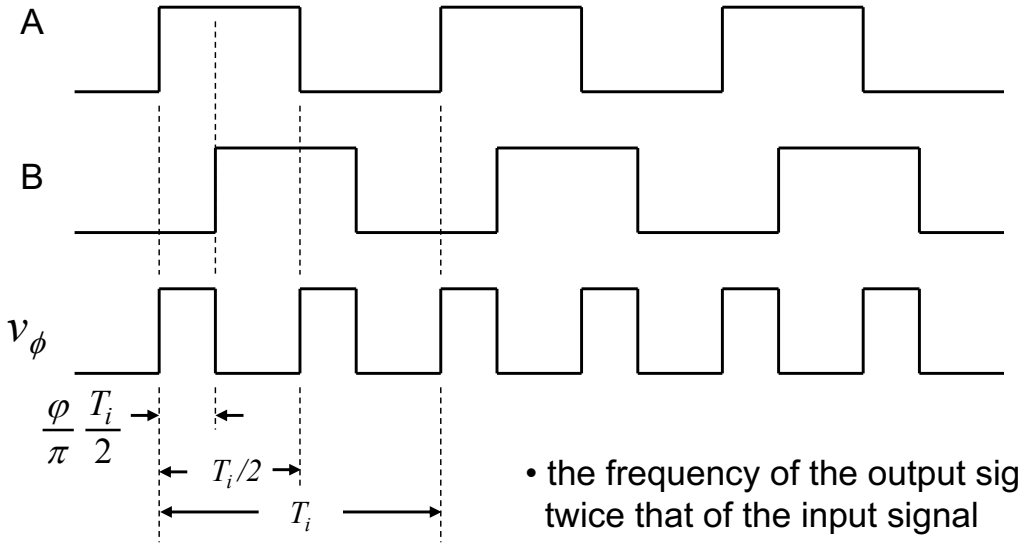
$$v(t) = A\cos(\omega t)\cos(\omega t + \phi) = \tfrac{A}{2}\cos(2\omega t) + \tfrac{A}{2}\cos(\phi)$$

- The 4046 allows the designer to choose between two different types of *digital* phase detectors (or phase comparators):
  - Phase Comparator I is an Exclusive OR gate.
  - Phase Comparator II is an edge-triggered network.
- Here, we will focus on the XOR-based phase detector
  - its main advantage is its relative insensitivity to noise!

Operation of an XOR Phase Detector



A	B	Out
0	0	0
0	1	1
1	0	1
1	1	0



- the frequency of the output signal is twice that of the input signal

Observations

- A and B must both be square waves with 50% duty cycles (and the same frequency, of course)
- The output of the phase detector is a square wave signal with frequency $2f_i$ and duty cycle

$$D_\varphi = \frac{\varphi}{\pi} \ .$$ Can you prove this?

- As a Fourier series,

$$v_\varphi(t) = v_o + \sum_{k=1}^{\infty} v_k \sin\left(4k\pi ft - \theta_k\right) \ .$$

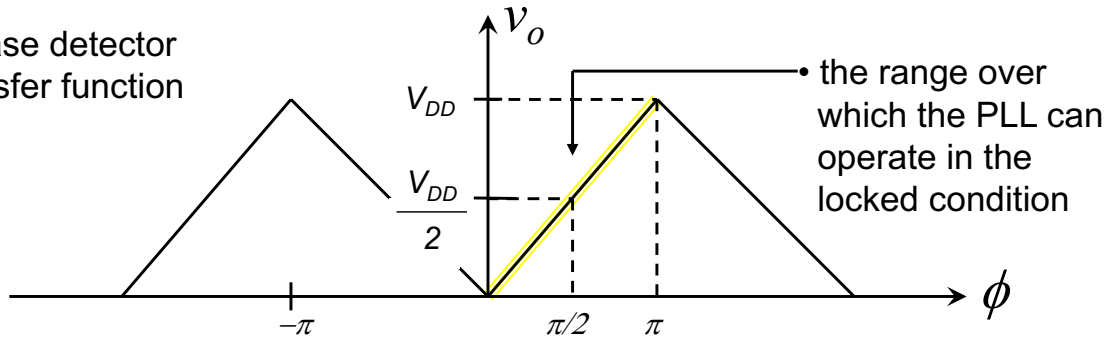
- v_0, the DC component of $v_\phi(t)$, is the average of $v_\phi(t)$ over a period of $T_i/2$.

$$v_0 = \frac{1}{T_i/2}\int_0^{T_i/2} v_\varphi(t)\,dt \quad = \frac{2}{T_i}\int_0^{D_\varphi T_i/2} V_{DD}\,dt$$

$$= \frac{V_{DD}}{\pi}\varphi \quad = K_D\varphi$$

K_D = the gain or sensitivity of the phase detector

Phase detector transfer function



- the range over which the PLL can operate in the locked condition

- Note that one cannot distinguish between positive and negative phase

4.3 Loop Filter

- The output v_ϕ of the phase detector is filtered by an external low-pass filter.
- Purpose: Pass DC and low-frequency components while attenuating high-frequency components @ $f = 2kf_i$
- The simple passive RC filter used in conjunction with the 4046 has the transfer function

$$F(s) = \frac{1}{1+sR_fC_f} = \frac{1}{1+s/\omega_p}$$

where $f_p = \frac{\omega_p}{2\pi} = \frac{1}{2\pi R_fC_f}$ = the cut-off frequency.

- The loop filter cannot completely eliminate the high frequency components; they show up as ripple on $v_o(t)$.

4.4 Voltage Controlled Oscillator

- The filter output v_c controls the frequency of the VCO
- The VCO output v_{osc} is a square wave with 50% duty cycle.
- The VCO transfer function is determined by three external components: *R1, R2*, and *C1*
- When v_c = 0, the VCO operates at

$$f_{\min} \approx \frac{1}{R_2(C_1 + 32\ \text{pF})}$$

- When $v_c = V_{DD}$, the VCO operates at

$$f_{\max} \approx f_{\min} + \frac{1}{R_2(C_1 + 32\ \text{pF})}$$

- These expressions are very approximate; the exact values for the components must be determined experimentally.

- Limitations on *R1, R2*, and *C1*

$$10\,\text{k}\Omega \le R_1 \le 1\,\text{M}\Omega$$

$$10\,\text{k}\Omega \le R_2 \le 1\,\text{M}\Omega$$

$$100\,\text{pF} \le C_1 \le 0.1\,\mu\text{F}$$

- For f_{osc} between f_{min} and f_{max}, $f_{osc}(v_c)$ is ideally a linear function of the control voltage v_c
- The slope $K_0 = \Delta f_{osc}/\Delta v_c$ is the gain or frequency sensitivity of the VCO in units of Hz/V.

4.5 Operation of the 4046 Phase-Locked Loop

4.5.1 No Incoming Signal, v_i = 0

- The VCO output v_{osc} is a square-wave signal with a 50% duty cycle
- The output of the XOR-based phase detector is "identical" to v_{osc} ($v_\phi = v_{osc}$)
- The DC component of $v_\phi = V_{DD}/2$.
- $f_{osc} = \dfrac{f_{\min} + f_{\max}}{2} = K\, v_\varphi,\ v_\varphi = V_{DD}/2.$

4.5.2 Incoming Signal @ f_i

- If f_i is sufficiently close to f_0, the phase-locked loop will lock onto it.
- How does the capture process work?

- During the capture process, the phase difference between v_i and v_{osc} changes with time
- Accordingly, v_c changes over time until it reaches the value required to set f_{osc} to f_i.
- In the locked condition,
  - $f_{osc} = f_i$
  - the reference and output signals are phase shifted by ϕ.
- The exact value of ϕ is that required to produce v_c that will set f_{osc} to f_i.

f_i	φ (rad)	v_0
f_{max}	π	V_{DD}
f_0	π/2	$V_{DD}/2$
f_{min}	0	0

4.6 Lock and Capture Ranges

- Once locked, the PLL remains locked as long as

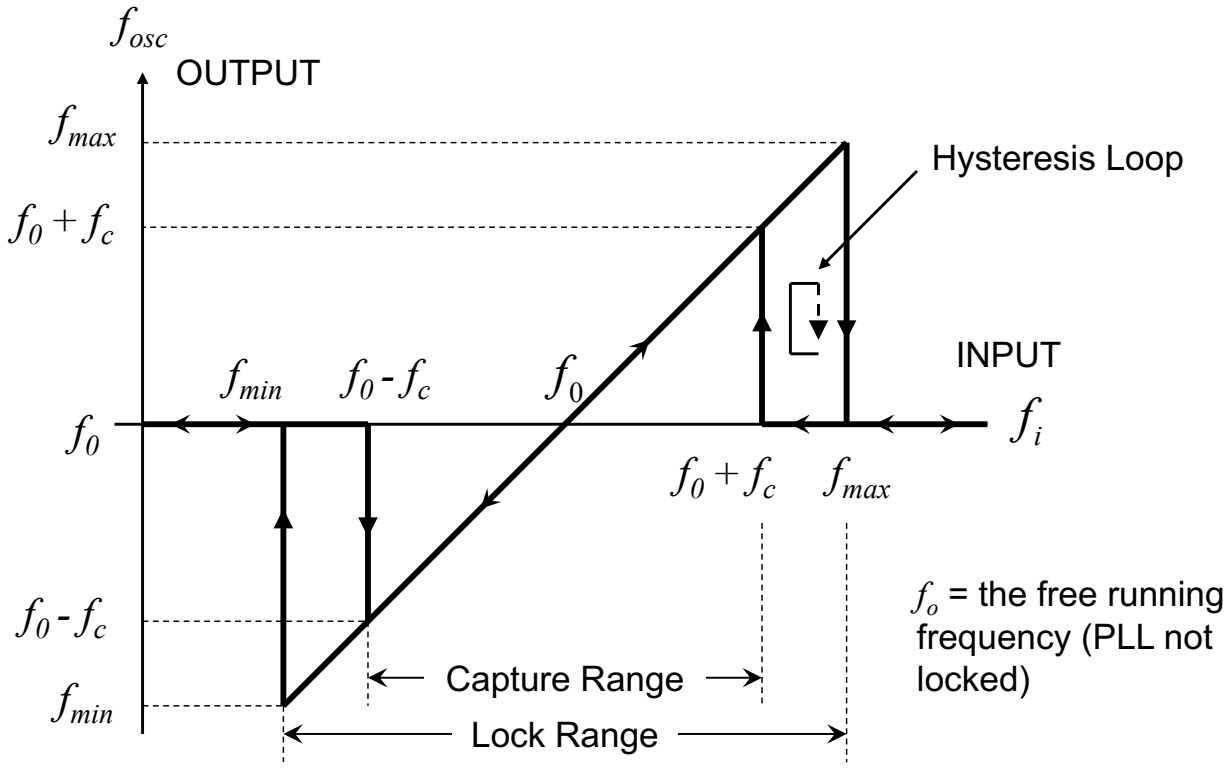
$$f_{\min} \le f_i \le f_{\max}$$

  where f_{max} - f_{min} is the lock range
- Once lock is lost, the VCO reverts to operation at the free-running frequency f_0.
- To establish lock again, f_i must be "sufficiently close" to f_0, *i.e.,*

$$f_0 - f_c \le f_i \le f_0 + f_c$$

  where 2 f_c is the capture range.

Tracking Characteristics of a Basic PLL



- The capture range $2f_c$ depends upon the characteristics of the loop filter.
- For the simple RC filter, a very crude and approximate expression for the capture range is

$$f_c \approx \frac{V_{DD}}{2} \frac{K_0}{\sqrt{1+(f_c / f_p)^2}}$$

where K_0 is the VCO gain (in units of Hz/V) and
f_p is the cut-off frequency of the filter.

- Given K_0 and f_p, this can be solved for f_c using numerical methods.
- The result is an approximate theoretical prediction for the capture range $2f_c$.

- If the capture range is much larger than the cut-off frequency of the filter

$$f_c / f_p \gg 1,$$

the expression for the capture range simplifies to

$$2f_c \approx \sqrt{2K_0 f_p V_{DD}}\ .$$

Observations

- The capture range $2f_c$ shrinks as the cut-off frequency f_p of the loop filter drops. This suggests that it would normally be advantageous to increase f_p in order to increase $2f_c$.
- However, it is also advantageous to lower f_p in order to:
  - better attenuate the high-frequency components of v_ϕ at the phase detector output
  - improve noise rejection
- Ultimately, the transient response of the PLL must also be considered. (The change in instantaneous frequency will generally not be a step function.)
- Thus loop filter design is a trade off.

Summary and Conclusions

- A phase-locked loop is a feedback control system that is based upon the *phase* of a signal rather than its *amplitude.*
- Through suitable configuration, PLLs can be used in a variety of roles including frequency synthesis, FM demodulation and motor speed control.
- Design, implementation and application of PLLs requires the skills of a circuit or RF designer, control systems engineer, and applications engineer.
- In the lab assignment, you will become familiar with the function and operation of PLLs and their individual components.
- This will prepare you for advanced study of PLLs, especially analysis of the transient response of a phase-locked loop using control systems methods.