EECE 481

MOS Basics – part 2

Lecture 3

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MOS Current - Review

In general, the saturation region is entered when either the channel is pinched-off or the carriers achieved velocity saturation.

$$\text{if } V_{DS} \geq \frac{(V_{GS} - V_T)\, E_c L}{(V_{GS} - V_T) + E_c L} \Rightarrow \text{saturation}$$

$$\text{if } V_{DS} < \frac{(V_{GS} - V_T)\, E_c L}{(V_{GS} - V_T) + E_c L} \Rightarrow \text{linear}$$

$$I_{DS} = W \upsilon_{sat} C_{ox} \frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_c L} \quad \text{saturation}$$

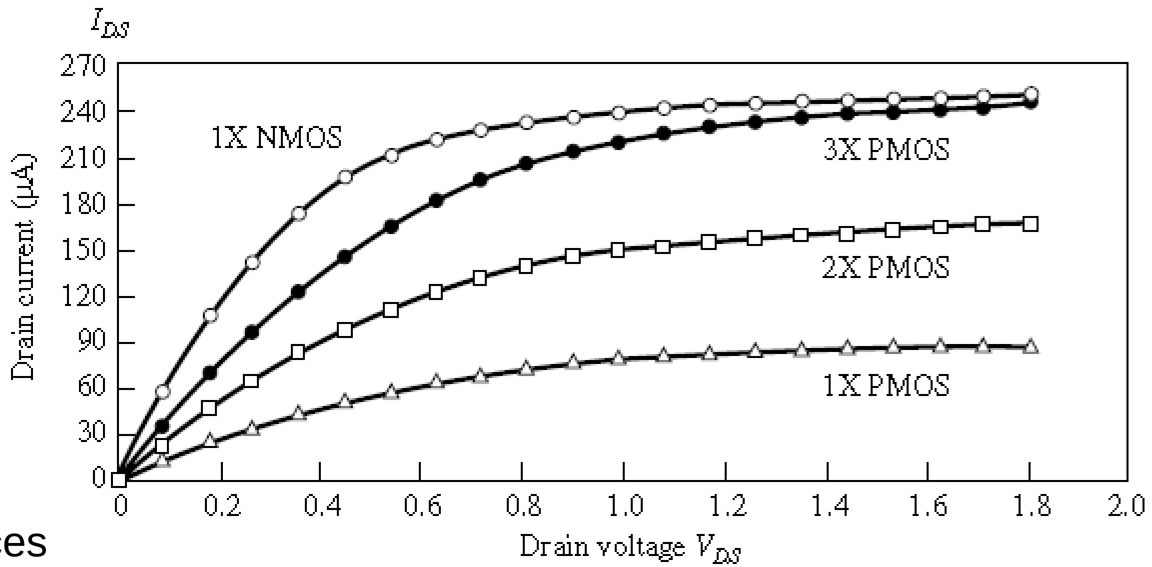
$$I_{DS} = \frac{W}{L} \cdot \frac{\mu_e C_{ox}}{\left(1 + \frac{V_{DS}}{E_c L}\right)} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \quad \text{linear}$$

Note that in extreme case ($E_c L >> V_{GS}$, V_{DS}) both equations translate to those of long channel devices

MOS Current – Short Channel Effects

The mobility of electrons is 4X higher than that of holes, i.e. in long channel regime the current of 1X NMOS is 4times a 1X PMOS

However, early velocity saturation of electrons makes this ratio smaller in short channel devices



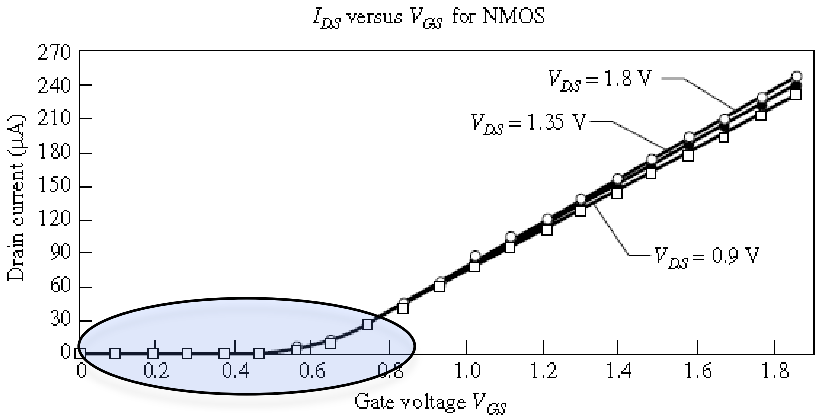
Current ratio of two 1X devices

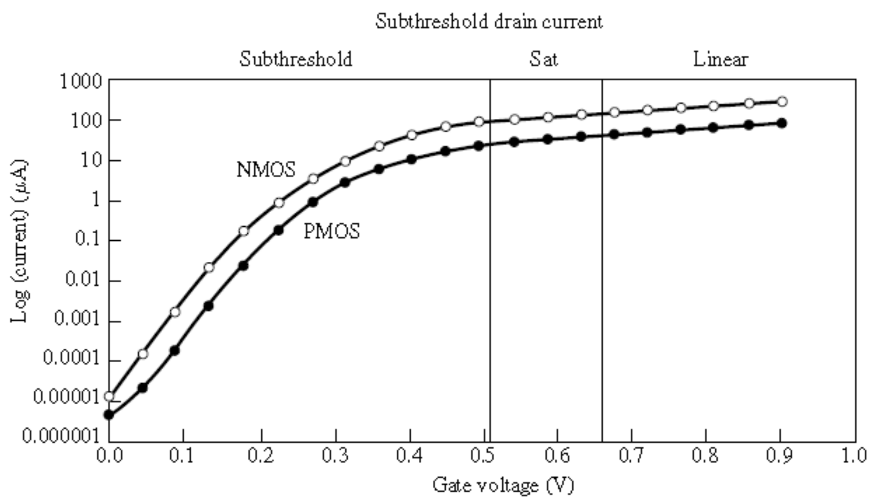
$$\frac{I_{DsatN}}{I_{DsatP}} = \frac{W_N\, \upsilon_{sat}\, C_{ox}\, (V_{GS} - V_{TN})^2/(V_{GS} - V_{TN} + E_{CN}L_N)}{W_P\, \upsilon_{sat}\, C_{ox}\, (V_{GS} - V_{TP})^2/(V_{GS} - V_{TP} + E_{CP}L_P)}$$

Roughly 2.4 for short channel devices

MOS Current - Sub threshold

Transistor turn-on/turn-off switching is a continuous process. At around V_{th} (and even below it) there is still significant leakage current.





$$I_{sub} = I_s e^{\frac{q(V_{GS} - V_T - V_{offset})}{nkT}} \left(1 - e^{\frac{-qV_{DS}}{kT}}\right)$$

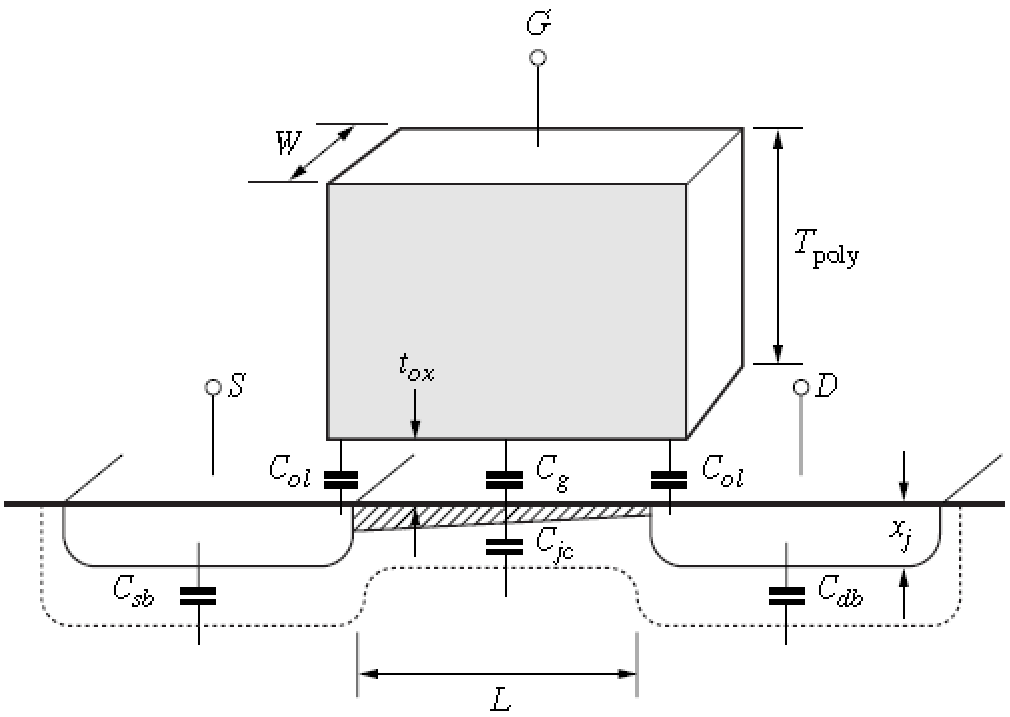
(Board Notes)

$$S = \Delta V_{GS} = \frac{nkT}{q} \ln(10)$$

slope factor

What is an ideal slope n and slope factor?

MOS Capacitances



- Each MOS device possess several junction and oxide capacitances (depends on dielectric and geometry) specified in units of fF/µm

- The charge/discharge of internal capacitances limits the switching speed

Gate (Oxide) Capacitance and DSM Evolution

$$C_G = WLC_{ox} = WL\frac{\varepsilon_{ox}}{t_{ox}} = WC_g$$

Gate Capacitance

5µm CMOS

$$C_g = C_{ox}L = \frac{\varepsilon_{ox}}{t_{ox}}L = \frac{(4)(8.85 \times 10^{-14})}{1100}(5\ \mu\text{m}) \cong 1.6\ \text{fF}/\mu\text{m}$$

0.35µm CMOS

$$C_g = C_{ox}L = \frac{\varepsilon_{ox}}{t_{ox}}L = \frac{(4)(8.85 \times 10^{-14})}{75}(0.35\ \mu\text{m}) \cong 1.6\ \text{fF}/\mu\text{m}$$

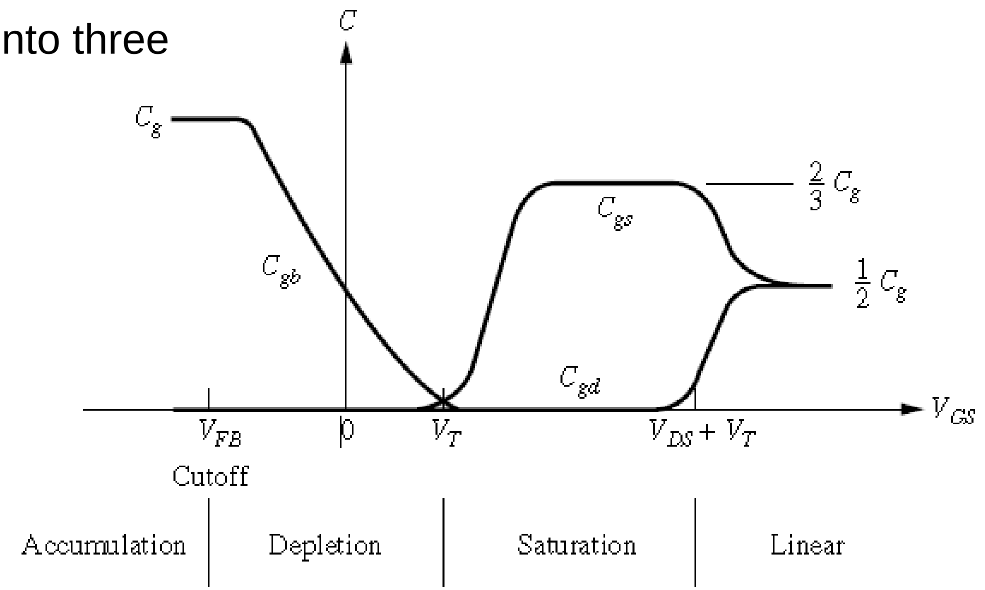
0.18µm CMOS

$$C_g = C_{ox}L = \frac{\varepsilon_{ox}}{t_{ox}}L = \frac{(4)(8.85 \times 10^{-14})}{22}(0.1\ \mu\text{m}) \cong 1.6\ \text{fF}/\mu\text{m}$$

The unit capacitance has remained constant over two decades! (part of constant field scaling plan introduced in 1970)

Gate Capacitance in different regions of operation

The total capacitace (Cg) is broken into three components C_{gb}, C_{gs} and C_{gd}



Why Does C_{gs} and C_{ds} change as we move from one region of operation to another?

(Board Notes)

	Cutoff	Linear	Saturation
C_{GS}	0	$\frac{1}{2} C_{ox}WL$	$\frac{2}{3} C_{ox}WL$
C_{GD}	0	$\frac{1}{2} C_{ox}WL$	0
C_{GB}	$C_{ox}WL$	0	0

Junction Capacitance

A *pn* junction when forward biased shows the following I-V characteristics

$$I_D = I_S(e^{V_J/V_{th}} - 1)$$

A *pn* junction when reverse-biased has a leakage current and a wider depletion region resulting in a voltage-dependant junction capacitor

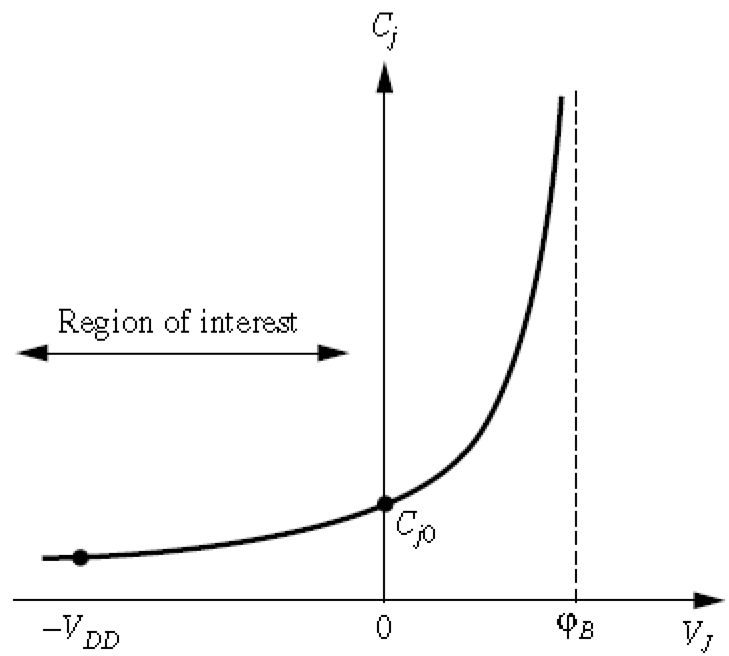
$$I_D = -I_S$$

$$C_J = \frac{C_{j0}\, A}{\left(1 - \frac{V_J}{\phi_B}\right)^m}$$

Capacitance of a *pn* junction

(in case of *abrupt* junction m=1/2)

(Board Notes)



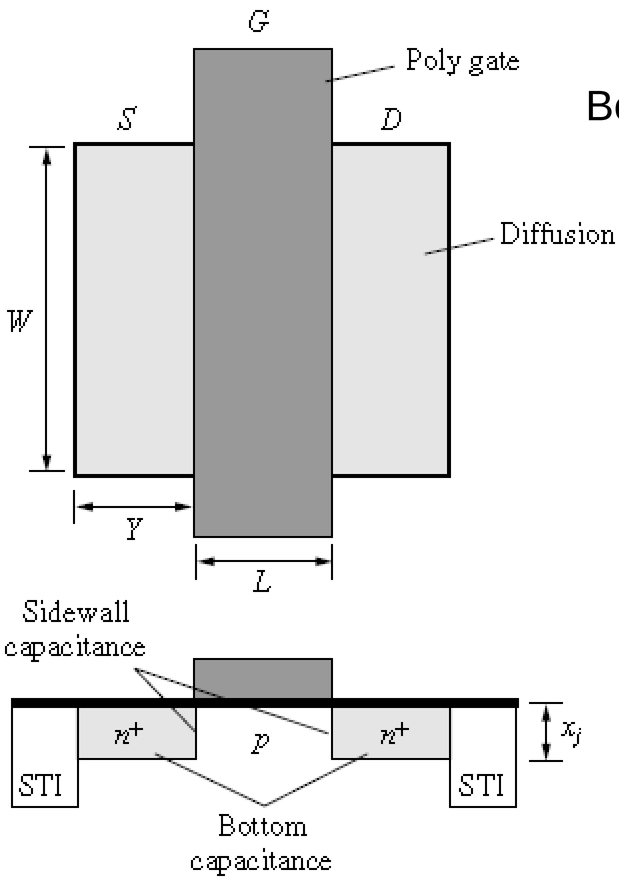
Junction capacitance vs junction potential

Diode (junction) built-in potential

$$\phi_B = \frac{kT}{q} \ln\left|\frac{N_A\, N_D}{n_i^2}\right.$$

$$C_{j0} = \sqrt{\frac{\varepsilon_{si} q}{2\phi_B} \frac{N_A N_D}{N_A + N_D}}$$

Junction Capacitance



$A_b = WY$

Bottom plate area

$A_{sw} = Wx_j$

Sidewall area

$$C_J = \frac{C_{jb}\,A_b}{\left(1 - \frac{V_J}{\phi_{Bb}}\right)^{mj}} + \frac{C_{jsw}\,A_{sw}}{\left(1 - \frac{V_J}{\phi_{Bsw}}\right)^{mjsw}}$$

If this is a voltage-dependant capacitance, how do model it as the device switches between different voltages?

1) Standard average (arithmetic mean)

2) Calculate the effective capacitance from $C_{eff} = \Delta Q / \Delta V$

$$C_{eq} = -\frac{C_{jb}\phi_B}{(V_2 - V_1)(1 - m)}\left[\left(1 - \frac{V_2}{\phi_B}\right)^{1-m} - \left(1 - \frac{V_1}{\phi_B}\right)^{1-m}\right]$$

(Board Notes)

Junction Capacitance - Example

Junction Capacitance Calculations

Problem:

(a) Find ϕ_B and C_{jb} for an n^+p junction diode with $N_D = 10^{20}\,\text{cm}^{-3}$ and $N_A = (3)10^{17}\,\text{cm}^{-3}$.

Solution:

From Equation (2.37),

$$\phi_B = \frac{kT}{q}\ln\frac{N_A N_D}{n_i^2} = 0.026\ \ln\left(\frac{3(10^{17})(10^{20})}{(1.45(10^{10}))^2}\right) = 1\ \text{V}$$

From Equation (2.39)

$$C_{jb} = \sqrt{\frac{\varepsilon_{si} q}{2\phi_B}\frac{N_A N_D}{N_A + N_D}} \approx \sqrt{\frac{\varepsilon_{si} q N_A}{2\phi_B}}$$

$$= \sqrt{\frac{11.7 * (8.85)(10^{-14}) * 1.6(10^{-19})(3)(10^{17})}{2(1.0)}} \approx 1.6\ \frac{\text{fF}}{\mu\text{m}^2}$$

Junction Capacitance – Example cont'd

Problem:

(b) For a 0.13 μm process, $W = 400$ nm, $L = 100$ nm, $x_j = 50$ nm, and the diffusion extension is $Y = 300$ nm. Using the layout of Figure 2.20, find C_j in units of fF for and $V_j = 0$ and $V_j = -1.2$ V.

Solution:

For $V_j = 0$, the value is obtained by multiplying C_{jb} with $(Y{+}x_j)W$

$$C_j = C_{jb}(Y + x_j)W = 1.6\,\text{fF}/\mu\text{m}^2 \times (0.3\,\mu\text{m} + 0.05\,\mu\text{m}) \times 0.4\,\mu\text{m} \approx 0.22\,\text{fF}$$

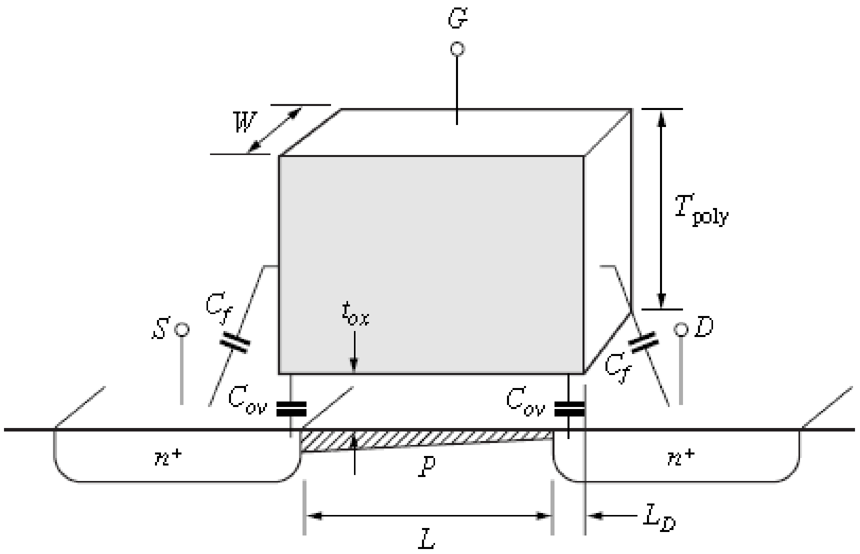
For $V_j = -1.2$,

$$C_j = \frac{C_{jb}(Y + x_j)W}{(1 - V_j/\phi_B)^m}$$

$$= \frac{1.6\,\text{fF}/\mu\text{m} \times (0.3\,\mu\text{m} + 0.05\,\mu\text{m}) \times 0.4\,\mu\text{m}}{(1 + 1.2/1.0)^{1/2}} = 0.16\,\text{fF}$$

Exercise: Use the integral (effective capacitance technique) and compare against the average here

Overlap Capacitance



-The lateral diffusion creates an overlap between gate and drain (source areas) creating a parasitic capacitance called *overlap* capacitance

- The proximity of drain (source) regions to the sidewall of gate in DSM contact creates another parasitic cap called *fringe* capacitance

$$C_f = \frac{2\varepsilon_{ox}}{\pi} \ln\left(1 + \frac{T_{poly}}{t_{ox}}\right)$$

$$C_{ol} = C_{ov} + C_f$$

$$C_{ov} = C_{ox} \times L_D$$

Summary

- The current capability ratio of NMOS and PMOS decreases (due to velocity saturation) as we move further into short channel regime.
- There is an exponential dependence of leakage current on V_{GS} in sub threshold region.
- A MOS device has three main physical types of capacitance
- The gate-oxide capacitance is re-distributed between source and drain, i.e. C_{GS} and C_{DS} vary, as device moves from linear to saturation region.
- The junction capacitance is voltage-dependant; we need to find an effective (average) capacitance for switching devices.
- The overlap/fringe capacitance becomes more important in DSM technologies.