EECE 481

Design of Resistive-Load Inverter
(Noise-margin-centric approach)
Lecture 5

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Multi Stage Noise Margin (MSNM) - Review

- Noise actually occurs between every gate and not at a single stage, as we have assumed so far

- In the above circuit, we need to determine how much noise we can tolerate before the circuit stops working as expected

- We note that $V_{out} = f(V_{in})$
- With noise $V_{out}' = f(V_{in}) + V_{noise} \times \text{Gain} + \text{Higher-order terms}$
- If the Gain $< 1$, then noise is attenuated; otherwise it is amplified
- IDEA: Develop a metric based on keeping the Gain $< 1$
Classical Noise Margin - Review

\[ \text{NM}_L = V_{IL} - V_{OL} \]

\[ \text{NM}_H = V_{OH} - V_{IH} \]
Requirements for a Valid Logic Gate - Review

- Must have a high gain region between two low gain regions
- Gain must be below 1 for low gain regions
- Gain must be greater than 1 for high gain region
- Output must swing from valid low to valid high
  - Low output should be below $V_{IL}$
  - High output should be above $V_{IH}$
Generic Structure of MOS inverters

• Basic structure of MOS inverter is shown below: NMOS pulldown device with a variety of possible pullup devices

![MOS Inverter Diagram]

• We will derive the noise margin parameters for different types of inverters
Resistive-Load Inverter Design
“5 Point Technique”

How to plot VTC from load line representation?

1) Find the two extremes of output voltage, e.g. $V_{OH}$ and $V_{OL}$ (be careful with the MOS region of operation for each derivation)

2) Express the $V_{out}$-$V_{in}$ relationship (usually the current equations of the devices provides that ) and find points where $\delta V_{out}/\delta V_{in} = -1$ ($V_{IH}$ and $V_{IL}$)

3) Find the switching point where $V_{in}=V_{out}=V_S$

4) Plot VTC using the values of five points and calculate NM as $V_{OH}-V_{IH}$ and $V_{IL}-V_{OL}$
Resistive-Load Inverter Design – cont’d

Let’s apply the technique to resistive-load inverter design

1) The extremes

Remember that in inverters an input value of $V_{OH}$ (it is the output of previous stage) creates an output of $V_{OL}$ and vice versa, hence we first find the easier of the two, i.e. the more straightforward one, and then replace it in expression of $I_{OUT}=I_{load}$ to find the other one

- At one extreme the transistor is off hence no current, $V_{OH}=V_{DD}$
- At the other extreme we use $V_{in}=V_{OH}=V_{DD}$ in the expression of $I_{OUT}=I_{load}$ to find the $V_{OL}$

$$I_R = I_{DS} \text{(lin)}$$

Substituting in the expressions for the resistor current and NMOS current:

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{W_N}{L_N} \cdot \frac{\mu_n C_{ox}}{2} \left[ 2 \left( V_{OH} - V_T \right) V_{OL} - V_{OL}^2 \right]$$

We know $V_{OL}$ is very small so for your calculations we can ignore it (Engineering approximations are IMPORTANT!)
Resistive-Load Inverter Design – cont’d

\[ \text{setting } k = (W/L) \mu_n C_{ox}: \]

\[ \frac{V_{DD} - V_{OL}}{R_L} = \frac{k}{2} \left[ 2(V_{OH} - V_T) V_{OL} - V_{OL}^2 \right] \]

Knowing that \( V_{OH} = V_{DD} \) and neglecting \( V_{OL}^2 \)

\[ V_{OL} \approx \frac{V_{DD}}{1 + kR_L(V_{DD} - V_T)} \]

Q: What should \( V_{OL} \) ideally be? What are the engineering trade-offs to make it happen?

Note that we always trade-off power, area, timing and noise margin versus one another

- Cost
- Performance

Board Notes
2. Now, let’s derive $V_{IL}$

Note that these values are now input voltages corresponding to $\delta V_{out}/\delta V_{in} = -1$

Step 1: detect the region of MOS operation

For $V_{IL}$ the input is still considered low and output voltage is near $V_{DD}$ (large $V_{DS}$)

$$I_R = I_{DS} (sat)$$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{W_{\nu_{sat}} C_{ox}(V_{in} - V_T)^2}{(V_{in} - V_T) + E_CL}$$

Use engineering intuition again: $V_{in} - V_T$ is small

Recalling that $\nu_{sat} = \mu E_C/2$

Setting $k = (W/L)\mu_{\nu} C_{OX}$

Now differentiate with respect to $V_{in}$, set $\delta V_{out}/\delta V_{in} = -1$, and $V_{in} = V_{IL}$

$$V_{IL} = V_T + \frac{1}{kR_L}$$
Let’s look at \( \text{NM}_L \) now:

\[
V_{IL} = V_T + \frac{1}{kR_L} \\
V_{OL} \approx \frac{V_{DD}}{1 + kR_L(V_{DD} - V_T)}
\]

Q: Do you see the problem with noise margin optimization? (change \( k \) and \( R_L \) to get a higher \( \text{NM}_L \))

Q: Which one would be a higher priority?

Board Notes
2. Now, let’s derive $V_{IH}$

Step 1: detect the region of MOS operation

For $V_{IH}$ the output voltage is near 0V, small $V_{DS}$, Linear region of operation

$$
\frac{W}{L} \frac{\mu C_{ox}}{1 + \frac{V_{out}}{E_{C/L}}} \left[ (V_{in} - V_T) V_{out} - \frac{V_{out}^2}{2} \right] = \frac{V_{DD} - V_{out}}{R_L}
$$

Simplification using Engineering intuition

$$
k \left[ (V_{in} - V_T) V_{out} - \frac{V_{out}^2}{2} \right] \approx \frac{V_{DD} - V_{out}}{R_L}
$$

Differentiation

$$
k \left[ (V_{in} - V_T) \frac{\partial V_{out}}{\partial V_{in}} + V_{out} - V_{out} \frac{\partial V_{out}}{\partial V_{in}} \right] = -\frac{1}{R_L} \frac{\partial V_{out}}{\partial V_{in}}
$$

What is $V_{out}$ here?

$$
V_{IH} = V_T + \sqrt{\frac{8V_{DD}}{3kR_L}} - \frac{1}{kR_L}
$$

$$
\frac{\partial V_{out}}{\partial V_{in}} = -1
$$

$$
V_{IH} = V_T + 2V_{out} - \frac{1}{kR_L}
$$
3. In order to complete the derivation and plot the VTC we only need \( V_S \) now (switching point)

Q: what is the MOS region of operation at switching point? Why?

\[
I_R = I_{DS} \quad \text{and} \quad V_{in} = V_{out} = V_S
\]

\[
\frac{W}{L} V_{sat} C_{ox} (V_S - V_T)^2 \left( V_S - V_T \right) + E_{CL} = \frac{V_{DD} - V_S}{R_L}
\]

Side discussion: How to solve higher-order equation?
- Deterministic equations
- Iteration technique
- SPICE