EECE 481

Design of CMOS Inverter
(Noise-margin-centric approach)
Lecture 6

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Resistive-load Inverter - Review

\[ V_{OH} = V_{DD} \]

\[ V_{OL} \approx \frac{V_{DD}}{1 + kR_L(V_{DD} - V_T)} \]

\[ V_{IH} = V_T + \sqrt{\frac{8V_{DD}}{3kR_L}} - \frac{1}{kR_L} \]

- Static power when the output is low
- Not straightforward to increase noise margin
- Large chip area to generate valid logic output
Saturated-enhancement-load Inverter

To alleviate the area problem we replace the resistor with a diode-connected transistor (always in saturation). This performance of this logic gate is affected by the ratio of devices, hence called *ratioed* inverter.

\[
K_R = \frac{k_{inert}}{k_{load}} = \frac{k'(W/L)_I}{k'(W/L)_L} = \frac{(W/L)_I}{(W/L)_L}
\]

The output voltage does not quite reach \( V_{DD} \) (The Load device requires at least VT drop on its \( V_{GS} \))

\[
V_{OH} = V_{DD} - V_T(V_{OH})
\]

\[
= V_{DD} - \left[ V_{T0} + \gamma(\sqrt{V_{OH}} + 2|\phi_F| - \sqrt{2|\phi_F|}) \right]
\]
To derive the $V_{OL}$ again it is important to find the proper region of operation for each transistor

$$I_{D_{L}}(\text{lin}) = I_{D_{L}}(\text{sat})$$

We can substitute in the current equations to obtain

$$\begin{align*}
V_{\text{in}} &= - \frac{W_{f}}{L_{f}} \frac{\mu_{n}C_{ox}}{1 + \frac{V_{\text{out}}}{E_{CN}L_{f}}} \left[ \left( V_{\text{in}} - V_{T} \right) V_{\text{out}} - \frac{V_{\text{out}}^{2}}{2} \right] = \frac{W_{f}V_{\text{sat}}C_{ox}(V_{DD} - V_{\text{out}} - V_{TL})^{2}}{(V_{DD} - V_{\text{out}} - V_{TL}) + E_{CN}L_{f}}
\end{align*}$$

Note that $V_{\text{in}}$ should be the output of previous stage (ideally $V_{DD} - V_{T}$), however, to keep things simple we occasionally assume $V_{\text{in}} = V_{DD}$ (see example 4.5)
To overcome the problem of low VOH in previous design, sometime a second supply voltage is used for the load device. Putting it in linear region of operation:

\[ V_{GG} > V_{DD} + V_{IL}(V_{DD}) \]

However, the name is no longer valid, for short-channel regime of operation. Why?
CMOS Inverter

- Address both issues of area and static power consumption
- Load that is complementary to the inverting device
- 5 distinct regions of operation can be detected
CMOS Inverter

Region II: NMOS saturation, PMOS Linear

V_{IL} falls in this region (why?)

\[
\frac{W_N v_{sat} C_{ox} (V_{in} - V_{TN})^2}{(V_{in} - V_{TN}) + E_{CN} L_N} = \frac{W_P}{L_P} \left( \frac{\mu_P C_{ox}}{1 + \frac{V_{DD} - V_{out}}{E_{CP} L_P}} \right) \\
\times \left[ (V_{DD} - V_{in} - |V_{TP}|)(V_{DD} - V_{out}) - \frac{(V_{DD} - V_{out})^2}{2} \right]
\]

(Board Notes)

\[
V_{IL} = \frac{2 V_{out} - V_{DD} - |V_{TP}| + (k_N/k_P)(V_{TN})}{1 + (k_N/k_P)}
\]
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Region III: NMOS saturation, PMOS saturation

\[ V_s \text{ falls in this region (why?)} \]

\[
\frac{W_N \nu_{sat} C_{ox}(V_S - V_{TN})^2}{(V_S - V_{TN}) + E_{CN}L_N} = \frac{W_P \nu_{sat} C_{ox}(V_{DD} - V_S - |V_{TP}|)^2}{(V_{DD} - V_S - |V_{TP}|) + E_{CP}L_P}
\]

(Board Notes)

\[
V_S = \frac{V_{DD} - |V_{TP}| + \chi V_{TN}}{1 + \chi}
\]

\[
\chi = \sqrt{\frac{W_N}{E_{CN}L_N} \frac{W_P}{E_{CP}L_P}} = \sqrt{\frac{\mu_n W_N}{\mu_p W_P}}
\]
CMOS Inverter

Region IV: NMOS linear, PMOS saturation

$V_{IH}$ falls in this region (why?)

$$
\frac{W_N}{L_N} \frac{\mu_r C_{ox}}{1 + \frac{V_{out}}{E_{CN} L_N}} \left[ (V_{in} - V_{TN}) V_{out} - \frac{V_{out}^2}{2} \right] = \frac{W_P v_{sat} C_{ox} (V_{DD} - V_{in} - |V_{TP}|)^2}{(V_{DD} - V_{in} - |V_{TP}|) + E_{CP} L_P}
$$

(Board Notes)

$$
V_{IH} = \frac{2V_{out} + V_{TN} + \left( k_P / k_N \right) (V_{DD} - |V_{TP}|)}{1 + \left( k_P / k_N \right)}
$$
CMOS Inverter - Layout

Note Minimum size, well-plugs, design rules