EECE 481

Design of CMOS Inverter

(Noise-margin-centric approach)

Lecture 6

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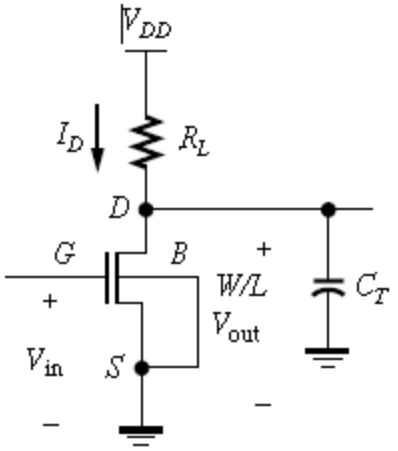
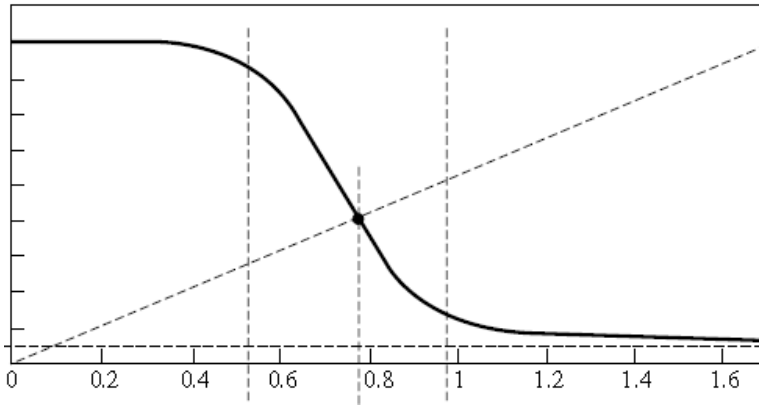
Resistive-load Inverter- Review





$$V_{OH} = V_{DD}$$

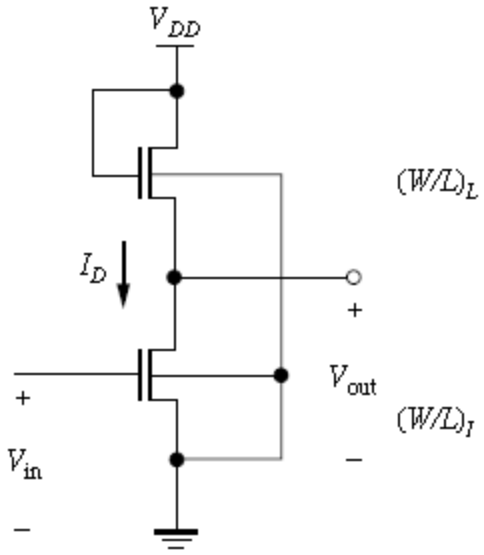
$$V_{OL} \approx \frac{V_{DD}}{1 + kR_L(V_{DD} - V_T)}$$

$$V_{IL} = V_T + \frac{1}{kR_L}$$

$$V_{IH} = V_T + \sqrt{\frac{8V_{DD}}{3kR_L}} - \frac{1}{kR_L}$$

- Static power when the output is low
- Not straightforward to increase noise margin
- Large chip area to generate valid logic output

Saturated-enhancement-load Inverter



To alleviate the area problem we replace the resistor

With a diode-connected transistor (always in saturation)

This performance of this logic gate is affected by the ratio

Of devices, hence called *ratioed* inverter

$$K_R = \frac{k_{\text{invert}}}{k_{\text{load}}} = \frac{k'(W/L)_I}{k'(W/L)_L} = \frac{(W/L)_I}{(W/L)_L}$$

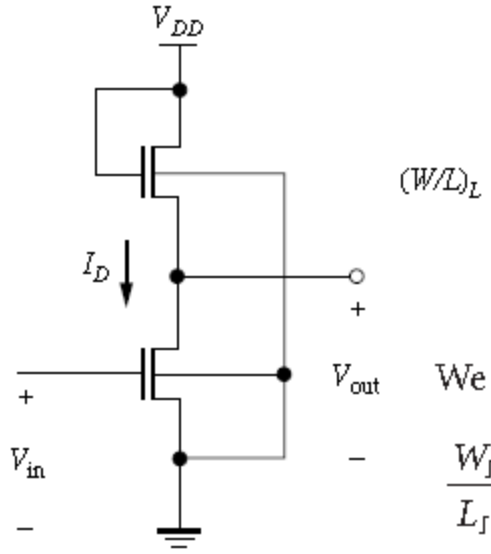
The output voltage does not quite reach V_{DD}

(The Load device requires at least VT drop on its V_{GS})

$$V_{OH} = V_{DD} - V_T(V_{OH})$$

$$= V_{DD} - [V_{T0} + \gamma(\sqrt{V_{OH} + 2|\phi_F|} - \sqrt{2|\phi_F|})]$$

Saturated-enhancement-load Inverter – cont'd



To derive the V_{OL} again it is important to find the proper region of operation for each transistor

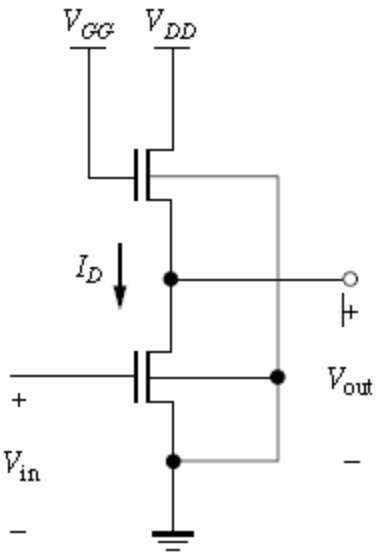
$$I_{DJ}(\text{lin}) = I_{DL}(\text{sat})$$

We can substitute in the current equations to obtain

$$\frac{W_J}{L_J}\frac{\mu_n C_{ox}}{\left(1+\dfrac{V_{\text{out}}}{E_{CN}L_J}\right)}\left[(V_{in}-V_{TJ})V_{\text{out}}-\frac{V_{\text{out}}^2}{2}\right]=\frac{W_L v_{sat}C_{ox}(V_{DD}-V_{\text{out}}-V_{TL})^2}{(V_{DD}-V_{\text{out}}-V_{TL})+E_{CN}L_L}$$

Note that V_{in} should be the output of previous stage (ideally $V_{DD} – V_T$), however, to keep Things simple we occasionally assume $V_{in} = V_{DD}$ (see example 4.5)

Linear-enhancement-load Inverter – cont'd



To overcome the problem of low VOH in previous design

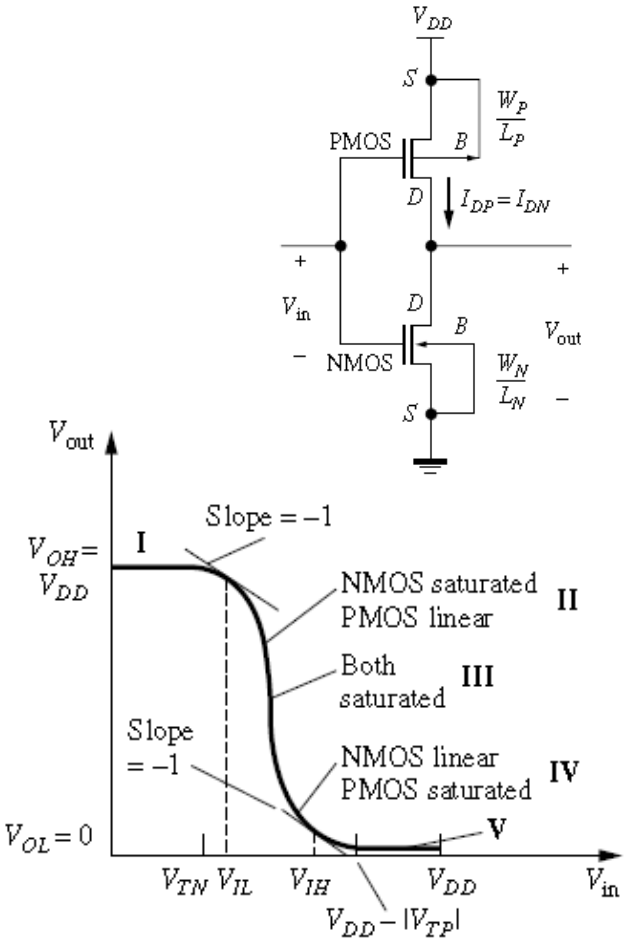
, sometime a second supply voltage is used for the load device

Putting it in linear region of operation

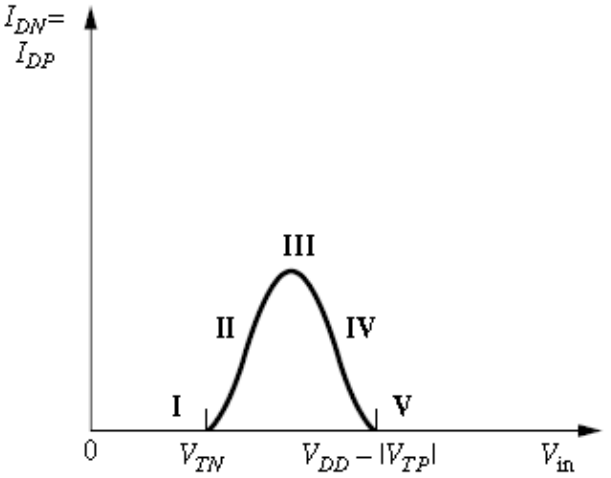
$$V_{GG} > V_{DD} + V_{TL}(V_{DD})$$

However, the name is no longer valid, for short-channel regime of operation. Why?

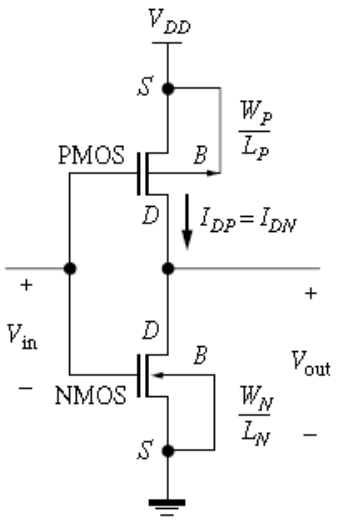
CMOS Inverter



- Address both issues of area and static power consumption
- Load that is complementary to the inverting device
- 5 distinct regions of operation can be detected



CMOS Inverter



Region II: NMOS saturation, PMOS Linear

V_{IL} falls in this region (why?)

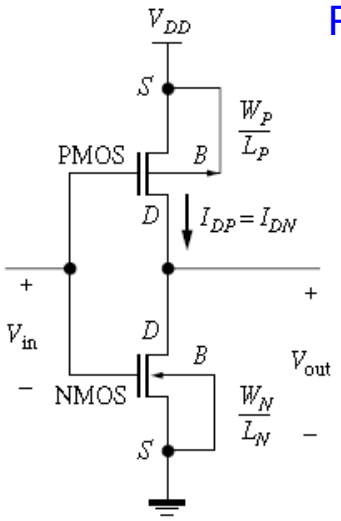
$$\frac{W_N \nu_{sat} C_{ox} (V_{in} - V_{TN})^2}{(V_{in} - V_{TN}) + E_{CN} L_N} = \frac{W_P}{L_P} \frac{\mu_p C_{ox}}{\left(1 + \frac{V_{DD} - V_{out}}{E_{CP} L_P}\right)}$$

$$\times \left[(V_{DD} - V_{in} - |V_{TP}|)(V_{DD} - V_{out}) - \frac{(V_{DD} - V_{out})^2}{2} \right]$$

(Board Notes)

$$V_{IL} = \frac{2V_{out} - V_{DD} - |V_{TP}| + (k_N/k_P)(V_{TN})}{1 + (k_N/k_P)}$$

CMOS Inverter



Region III: NMOS saturation, PMOS saturation

V_s falls in this region (why?)

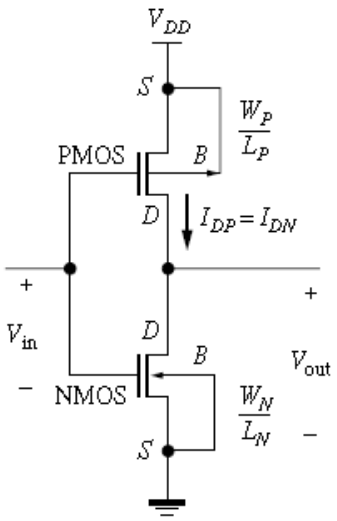
$$\frac{W_N \upsilon_{sat} C_{ox}(V_S - V_{TN})^2}{(V_S - V_{TN}) + E_{CN} L_N} = \frac{W_P \upsilon_{sat} C_{ox}(V_{DD} - V_S - |V_{TP}|)^2}{(V_{DD} - V_S - |V_{TP}|) + E_{CP} L_P}$$

(Board Notes)

$$V_S = \frac{V_{DD} - |V_{TP}| + \chi V_{TN}}{1 + \chi}$$

$$\chi = \sqrt{\frac{\frac{W_N}{E_{CN} L_N}}{\frac{W_P}{E_{CP} L_P}}} = \sqrt{\frac{\mu_n W_N}{\mu_p W_P}}$$

CMOS Inverter



Region IV: NMOS linear, PMOS saturation

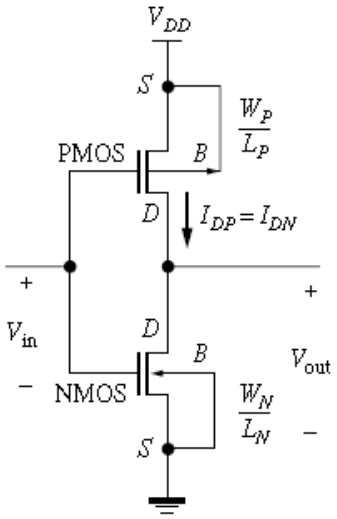
V_{IH} falls in this region (why?)

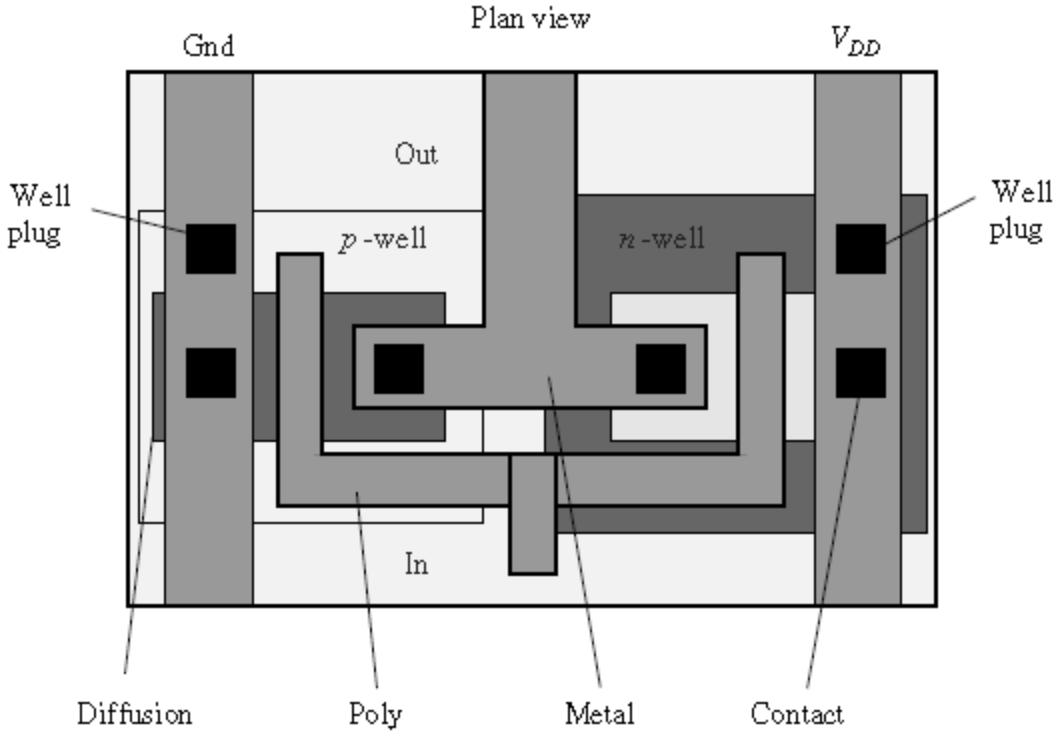
$$\frac{W_N}{L_N}\frac{\mu_n C_{ox}}{\left(1+\frac{V_{out}}{E_{CN}L_N}\right)}\left[(V_{in}-V_{TN})V_{out}-\frac{V_{out}^2}{2}\right]=\frac{W_P v_{sat} C_{ox}(V_{DD}-V_{in}-|V_{TP}|)^2}{(V_{DD}-V_{in}-|V_{TP}|)+E_{CP}L_P}$$

(Board Notes)

$$V_{IH}=\frac{2V_{out}+V_{TN}+(k_P/k_N)(V_{DD}-|V_{TP}|)}{1+(k_P/k_N)}$$

CMOS Inverter - Layout





Note Minimum size, well-plugs, design rules