EECE 481

CMOS Gates

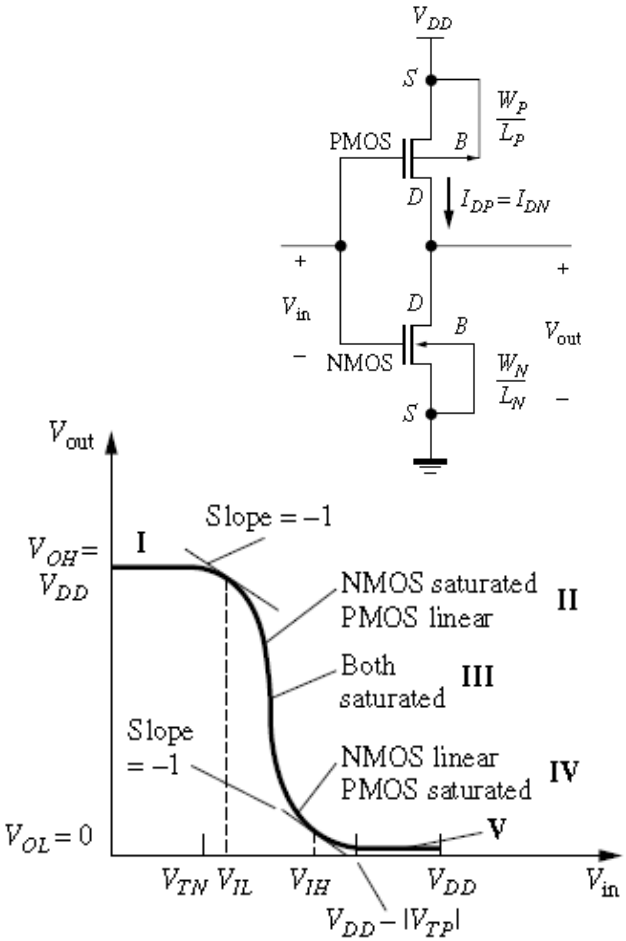
(VTC and Sizing)

Lecture 7

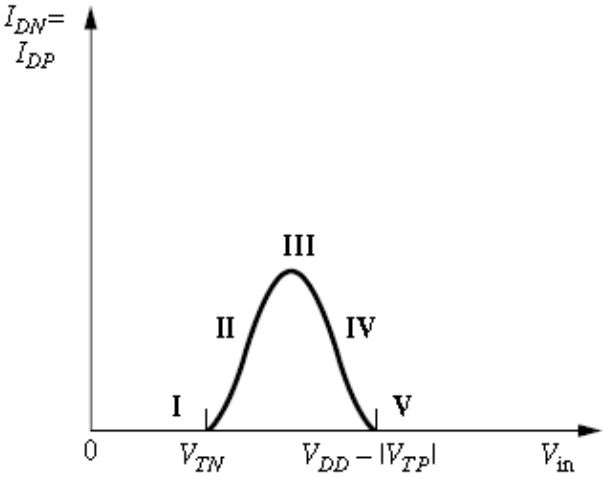
Reza Molavi
Dept. of ECE
University of British Columbia
reza@ece.ubc.ca

Slides Courtesy : Dr. Res Saleh (UBC), Dr. D. Sengupta (AMD), Dr. B. Razavi (UCLA)

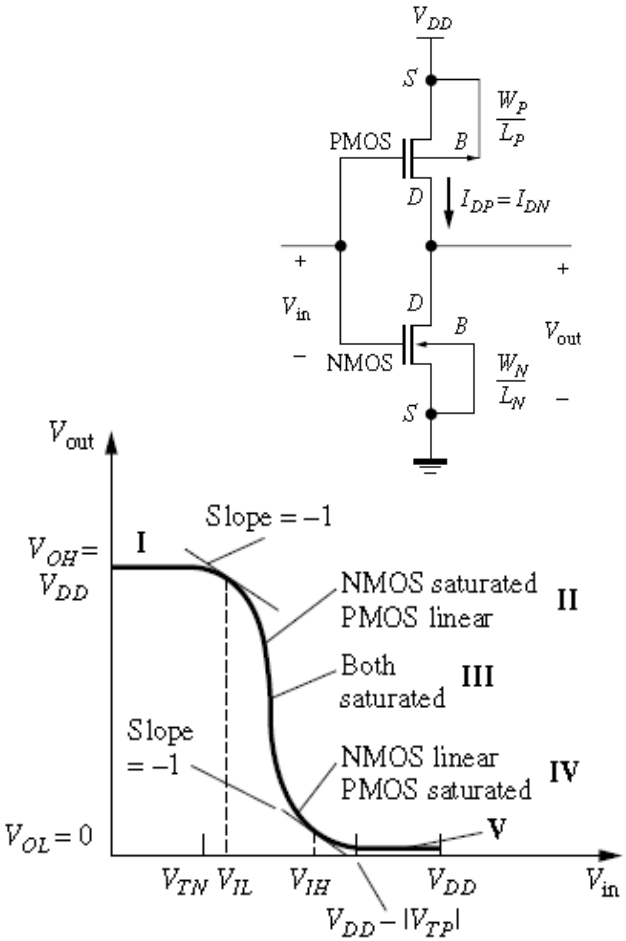
CMOS Inverter - Review



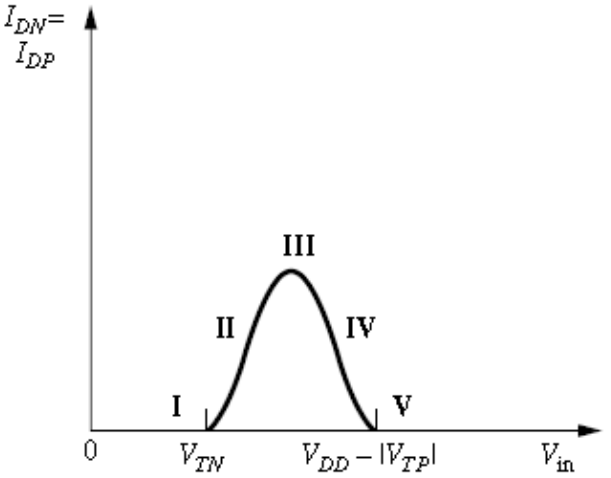
- Address both issues of area and static power consumption
- Load that is complementary to the inverting device
- 5 distinct regions of operation can be detected



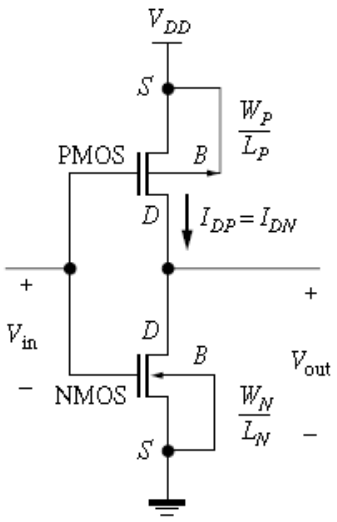
CMOS Inverter - Review



- Address both issues of area and static power consumption
- Load that is complementary to the inverting device
- 5 distinct regions of operation can be detected



CMOS Inverter - Review



Region II: NMOS saturation, PMOS Linear

$$V_{IL} = \frac{2V_{out} - V_{DD} - |V_{TP}| + (k_N/k_P)(V_{TN})}{1 + (k_N/k_P)}$$

Region III: NMOS saturation, PMOS saturation

$$\chi = \sqrt{\frac{\frac{W_N}{E_{CN}L_N}}{\frac{W_P}{E_{CP}L_P}}} = \sqrt{\frac{\mu_n W_N}{\mu_p W_P}}$$

$$V_S = \frac{V_{DD} - |V_{TP}| + \chi V_{TN}}{1 + \chi}$$

*Note: As we increase X, we make the NMOS side stronger (relative to PMOS), moving the VTC switching point to the left), We also showed that mathematically $\delta V_S / \delta X < 0$ to confirm the intuition

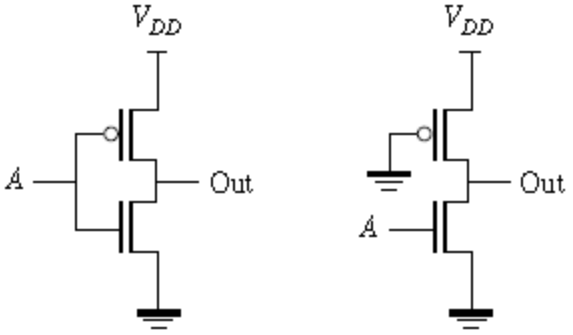
Region IV: NMOS linear, PMOS saturation

$$V_{IH} = \frac{2V_{out} + V_{TN} + (k_P/k_N)(V_{DD} - |V_{TP}|)}{1 + (k_P/k_N)}$$

Pseudo-NMOS Inverter

To address issues with NMOS loads

- Saturated NMOS load, a.k.a diode connected load, has degraded V_{OH}
- Linear NMOS load requires two supplies and extra area/interconnects
- CMOS gates require multiple loads for multi fanin inputs (?)



Solves the abovementioned problems, However

-*Ratioed* inverter, i.e. V_{OL} a function of two device ratios

- Large T_{PLH} (why?)

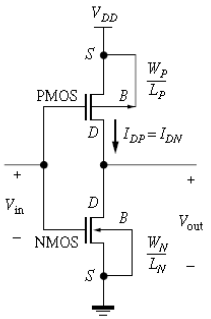
$$I_{DP}(\text{sat}) = I_{DN}(\text{lin})$$

$$\frac{W_P v_{sat} C_{ox}(V_{DD} - |V_{TP}|)^2}{(V_{DD} - |V_{TP}|) + E_{CP}L_P} = \frac{W_N}{L_N}\frac{\mu_n C_{ox}}{\left(1 + \frac{V_{OL}}{E_{CN}L_N}\right)}\left[(V_{DD} - V_{TN})(V_{OL}) - \frac{(V_{OL})^2}{2}\right] \Rightarrow V_{OL} = \frac{I_{DP}(\text{sat})}{k_N(V_{DD} - V_{TN})}$$

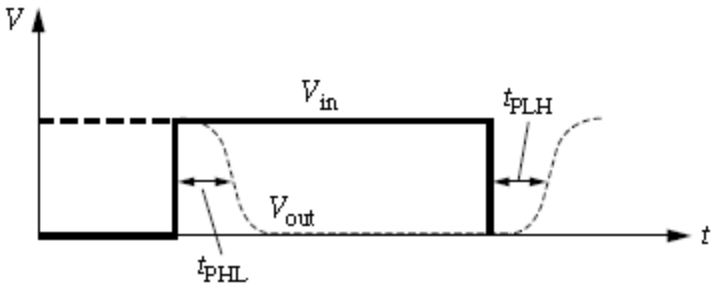
Inverter - Sizing

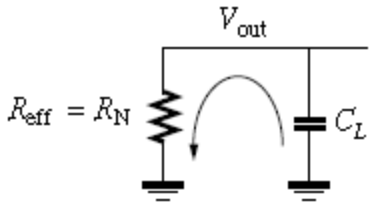
- In ratioed logic families (such as diode-connected load or pseudo NMOS, V_{OL} is a priority so the Size of load is mainly determined by the choice of V_{OL}

- In non-ratioed logic families (such CMOS inverters) propagation delay is important



Speed





Pull-down (output capacitor discharge)

through the NMOS transistor

$$V_{out}(t) = V_{DD}\, e^{-t/R_N C_L}$$

T_{PHL} is the time it take for the capacitor to discharge to 50% of the final value

(Board notes)

Inverter – Sizing II

-The value of T_{PHL} or T_{PLH} determine the value of the resistor (average on-resistance)

• Note that in the pull-down case (NMOS on) device starts in saturation (V_{DD} across its V_{DS} and might enter triode at some point, therefore it makes sense to define an effective resistance

$$R_{eqn} = 12.5\ \text{k}\Omega/\square$$

$$R_{eqp} = 30\ \text{k}\Omega/\square$$

Unit resistance of the devices (per square)

That is for a device with L=W (obtained from HSPICE simulation), note the ration 2.4, does It remind of a number?

$$R_N = R_{eqn} \times \frac{L_N}{W_N}$$

$$R_p = R_{eqp} \times \frac{L_p}{W_p}$$

Total Resistance inversely proportional to W/L (remember that in triode region we could model the transistor simply with a resistor!

Review Example 4.9 of textbook

Summary

- Resistive load inverter has a challenging trade-off among different design criteria such noise margin, area and power
- Diode-connected inverter is *ratioed* and suffers from degraded V
- Linear NMOS load is *ratioed* and suffers from large area and several power connections
-CMOS Inverter is not ratioed, has low power consumption and can be optimized for cerain propagation delay, however suffers from several loads when used for multi input gates
-Pseudo-NMOS Inverter is *ratioed,* uses single PMOS load and may have large propagation delay

- Going forward our focus will be on CMOS Gates

_ Let's Review HSPICE tutorial now!