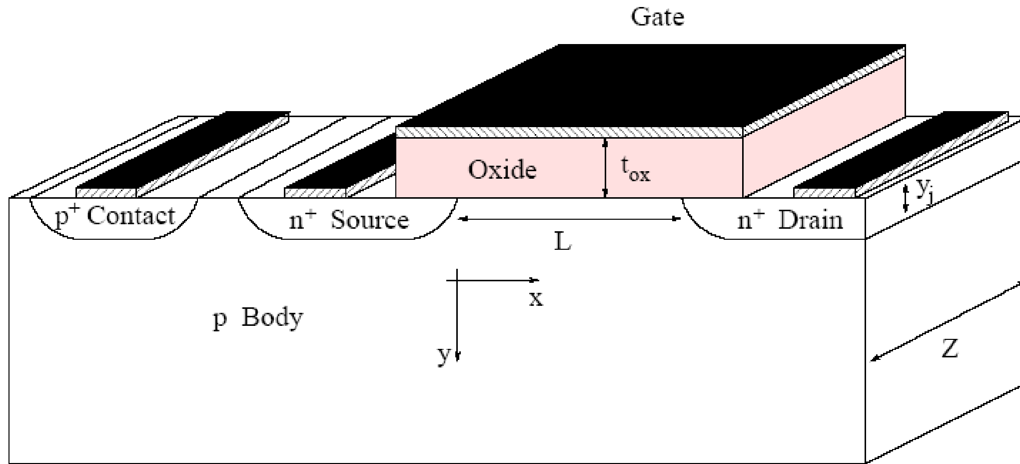
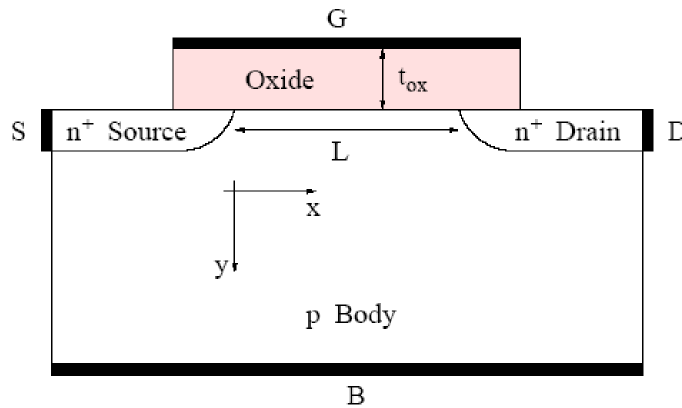
MOSFET small-signal equivalent circuits

LECTURE 16

- Short explanation of MOSFET I-V
- More MOSFET capacitance
- MOSFET small-signal equivalent circuits
- 2-port parameters
- y for intrinsic
- z for extrinsic
- s for HF
- power gains: MAG, MSG, U

Si MOSFET features





- 4 terminals
- 2D-device
- "The most abundant object made by mankind"

MOSFET surface potential

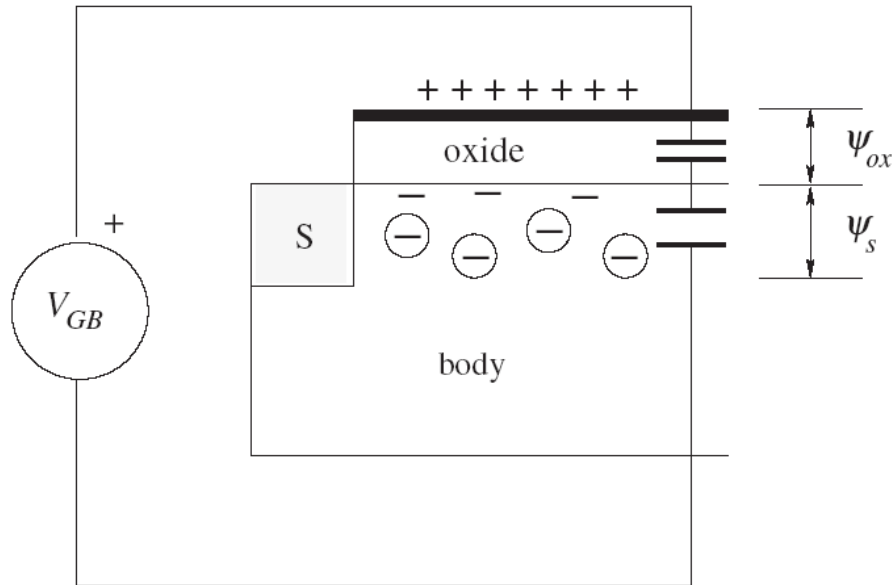


Figure 10.3 Representation of the oxide and the electrons and ions in the semiconductor as capacitors, for the purpose of determining the surface potential.

$$\Delta\psi_s = \Delta V_{GB}\frac{1}{1 + C_s/C_{ox}}$$

$$C_{ox} = -\frac{\Delta Q_s}{\Delta\psi_{ox}} \equiv \frac{\epsilon_{ox}}{t_{ox}} \quad \text{and} \quad C_s = -\frac{\Delta Q_s}{\Delta\psi_s}$$

MOSFET gate characteristic

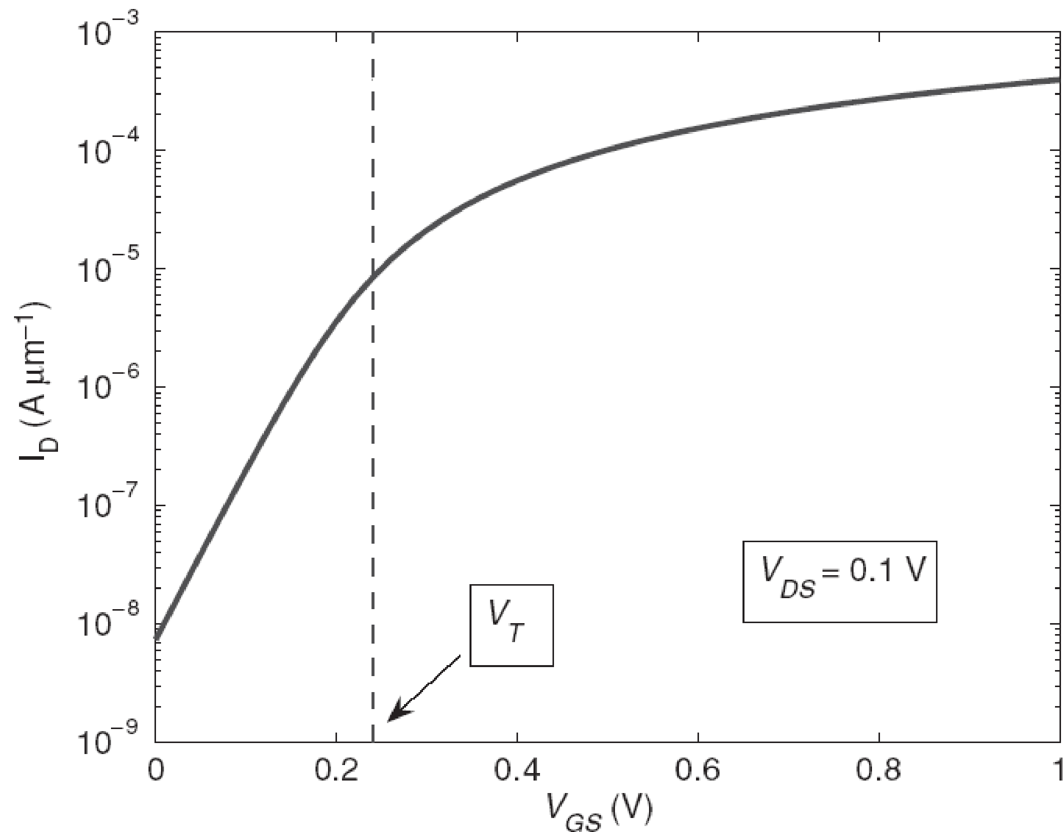


Figure 10.2 Transfer (or gate) characteristic at $V_{DS} = 0.1$ V for a CMOS90 NFET with the properties listed in Appendix C. The threshold voltage is 0.24 V. MEDICI (Synopsys) simulation using the DDE version of (5.24).

Sec. 10.1

MOSFET drain characteristic: above threshold

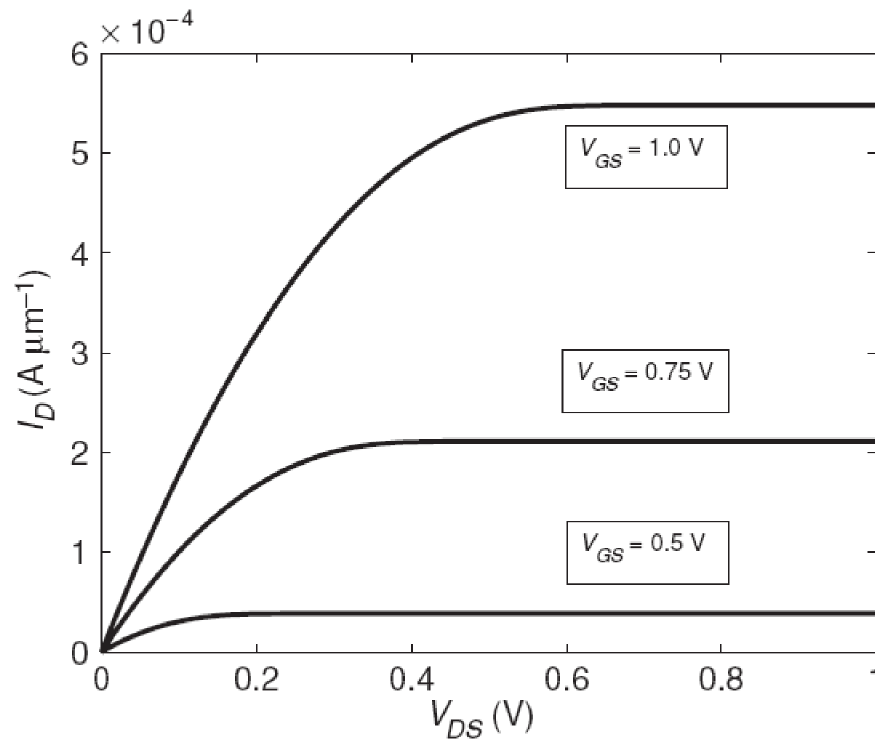
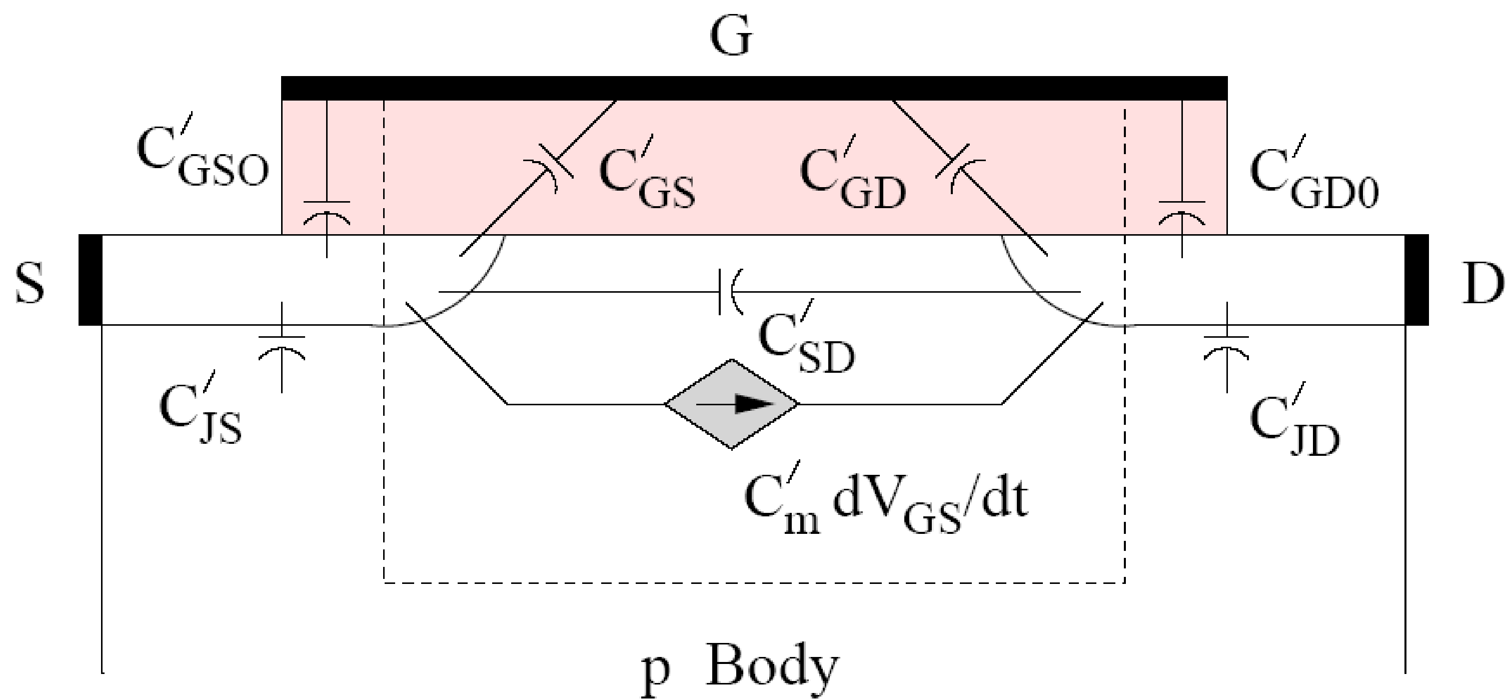


Figure 10.10 MOSFET drain characteristic from the surface potential model. Note: $V_{SB} = 0$, so that $V_{GS} \equiv V_{GB}$ and $V_{DS} \equiv V_{DB}$. Model parameters as given in Appendix C for a CMOS90 N-FET.

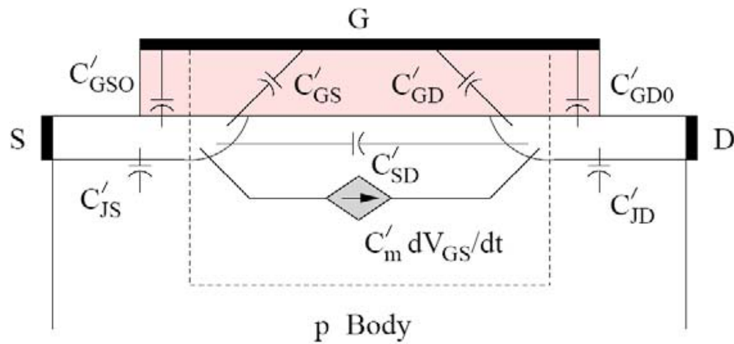
Sec. 12.2

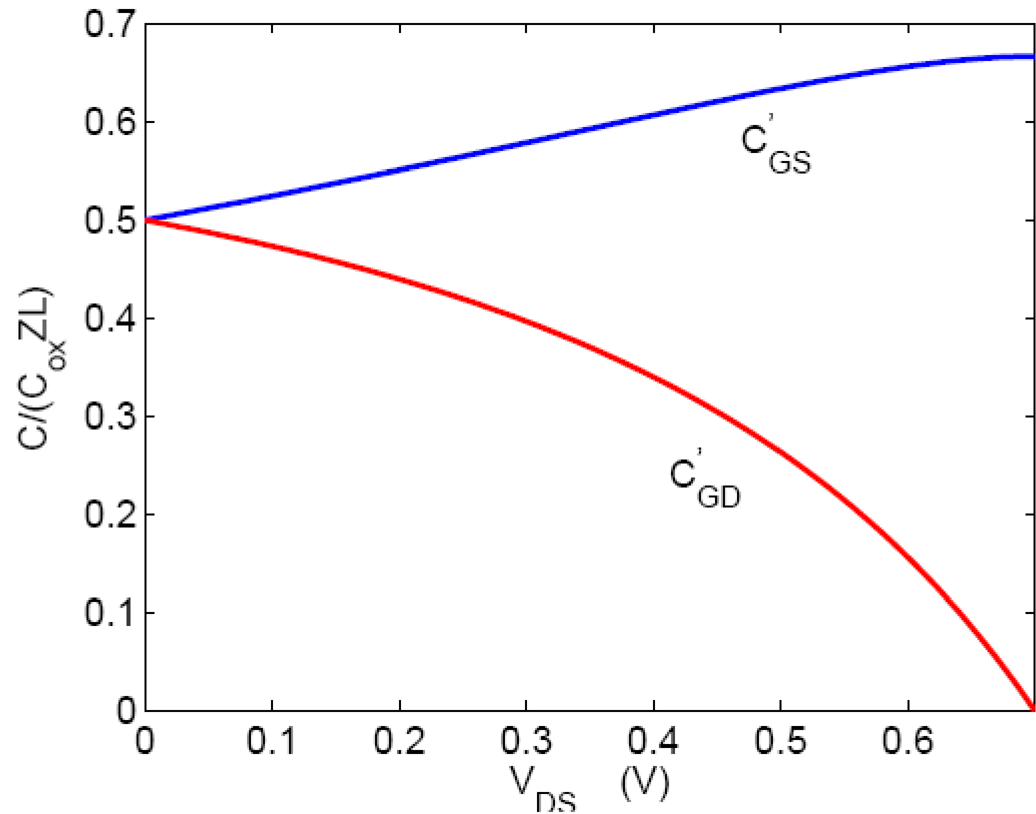
MOSFET capacitance



Sec. 12.2.1

Intrinsic capacitances and C_{ox}

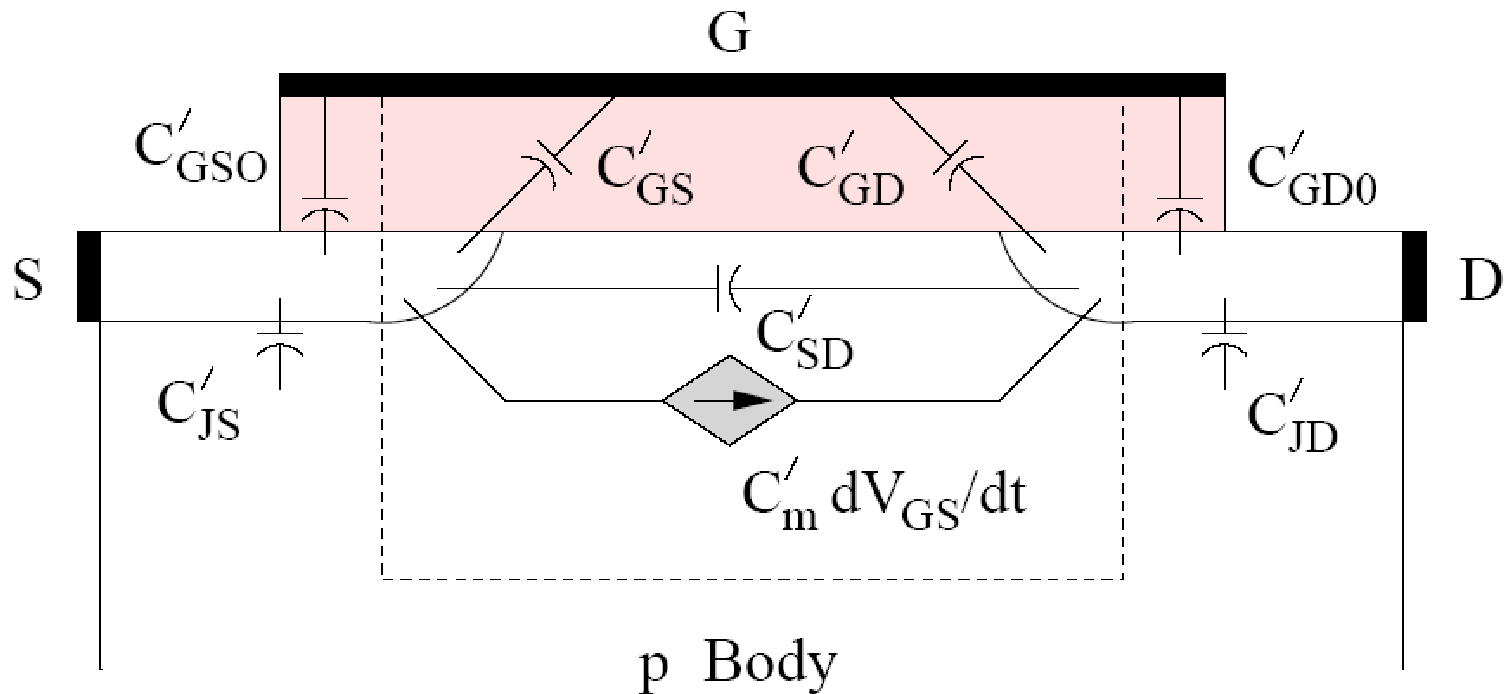




What are the reasons for these trends?

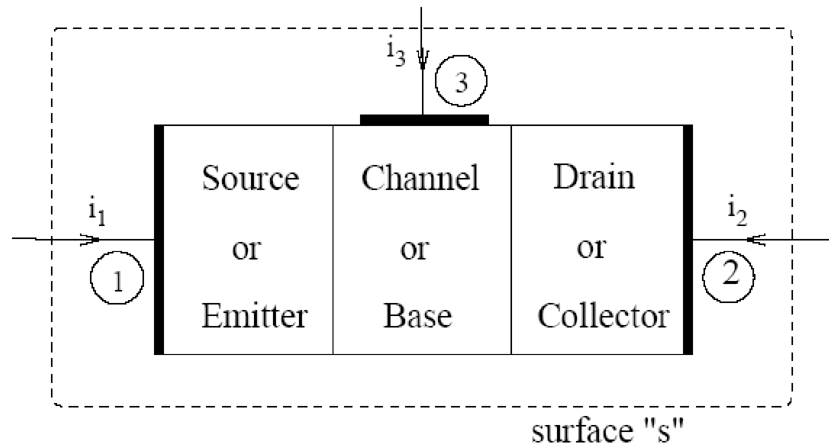
Sec. 12.3.1

Extrinsic MOSFET capacitance



Are the extrinsic capacitances reciprocal?

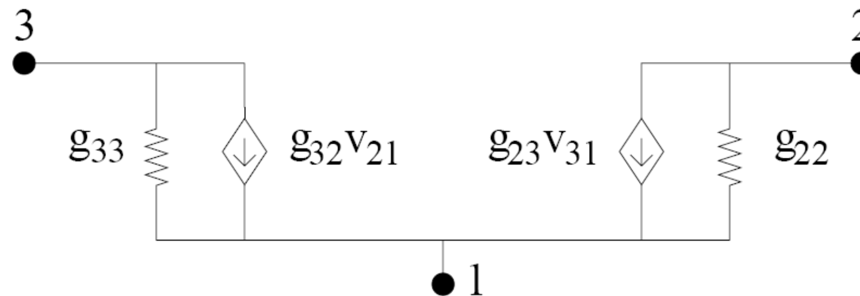
MOSFET small-signal conductance



Linearized expressions:

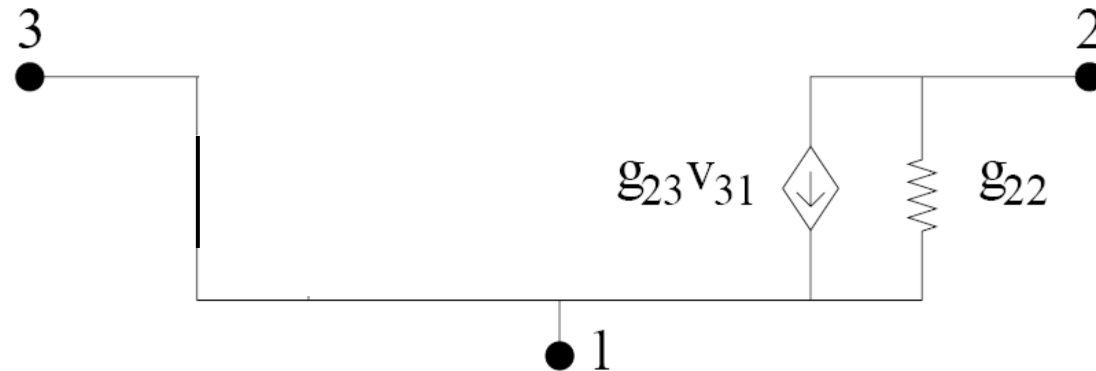
$$
\begin{aligned}
i_2 &= I_2(V_{21} + v_{21},\ V_{31} + v_{31}) \\
&= I_2(V_{21}, V_{31}) + \frac{\partial I_2}{\partial V_{21}} v_{21} + \frac{\partial I_2}{\partial V_{31}} v_{31} \\
&\equiv I_2 + g_{22} v_{21} + g_{23} v_{31} \, ,
\end{aligned}
$$

$$
\begin{aligned}
i_3 &= \frac{\partial I_3}{\partial V_{31}} v_{31} + \frac{\partial I_3}{\partial V_{21}} v_{21} \\
&= g_{33} v_{31} + g_{32} v_{21} \, ,
\end{aligned}
$$



Sec. 14.2

MOSFET conductance equivalent circuit



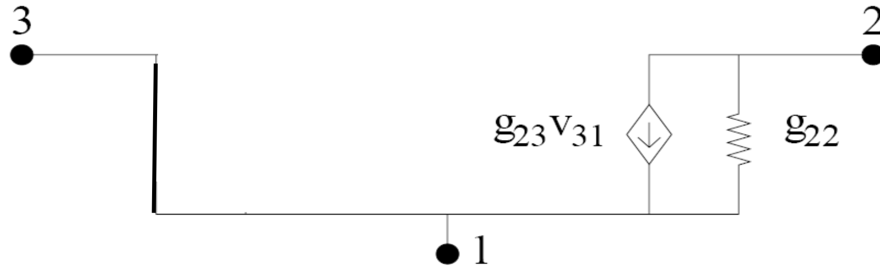
Why can g_{32} be ignored for MOSFETs?

When is it OK to ignore g_{GG} ?

What are the other conductances called?

Sec. 14.2

Linearized, hybrid-π circuit



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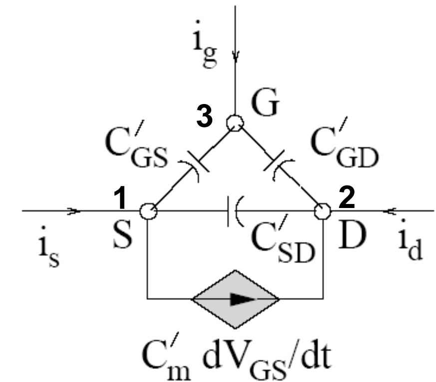

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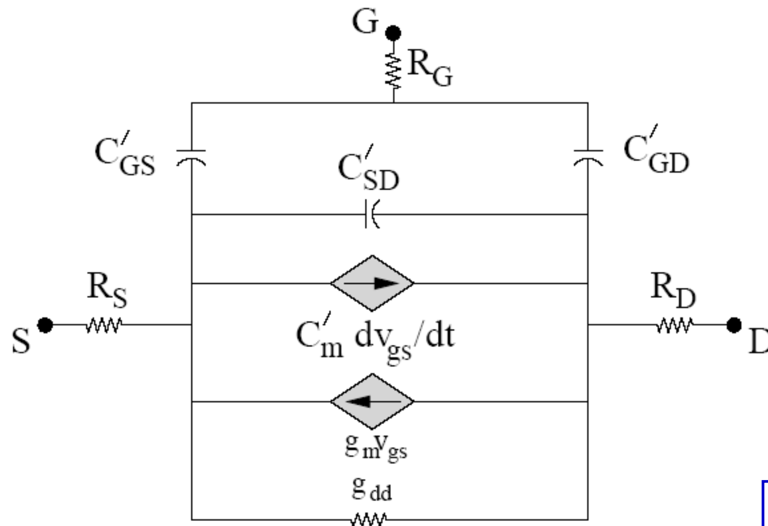

Can you see a π in the equivalent circuit?

Parasitic R's have been added

What is missing from this circuit?

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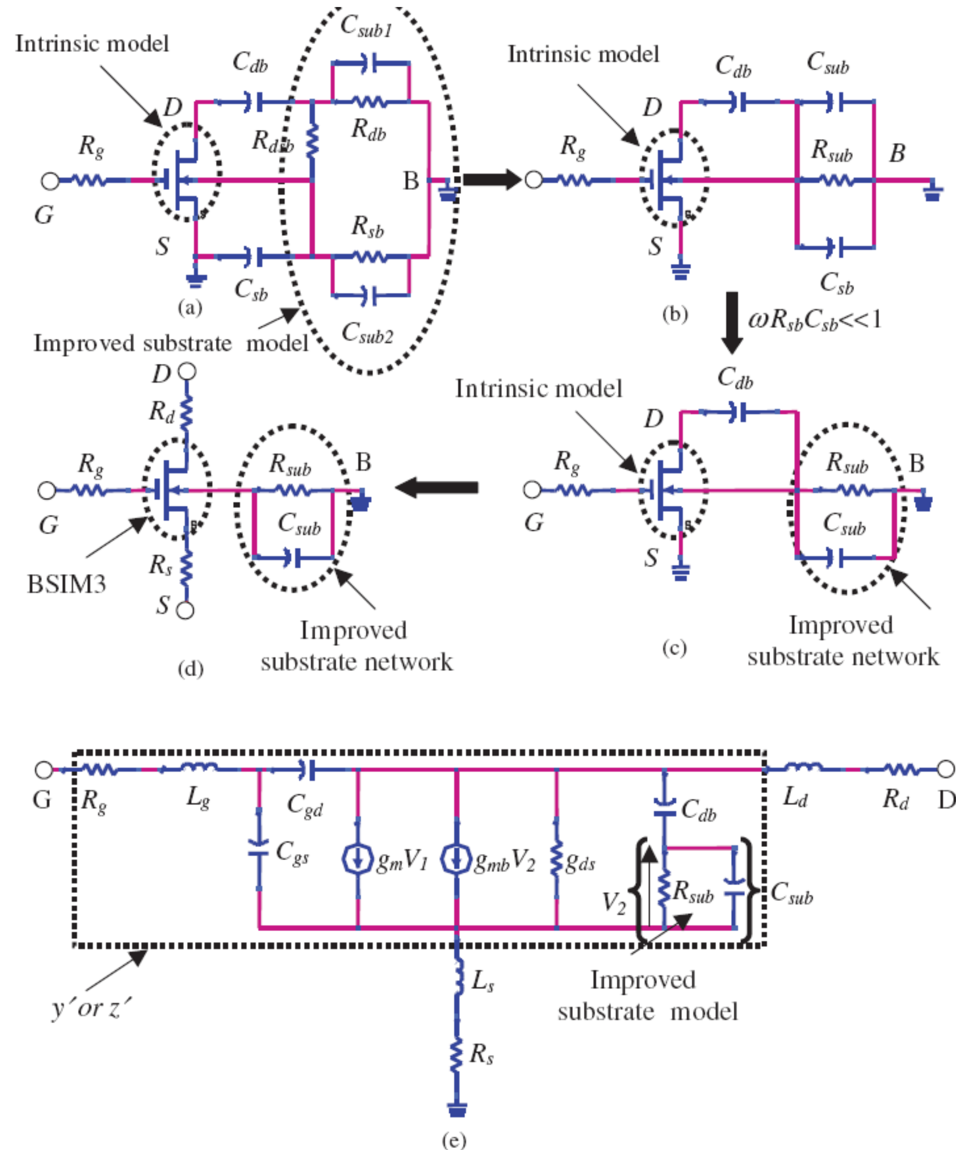
Int. J. Numer. Model. 2006; **19**:257–269
Published online in Wiley InterScience (www.interscience.wiley.com). DOI: 10.1002/jnm.610

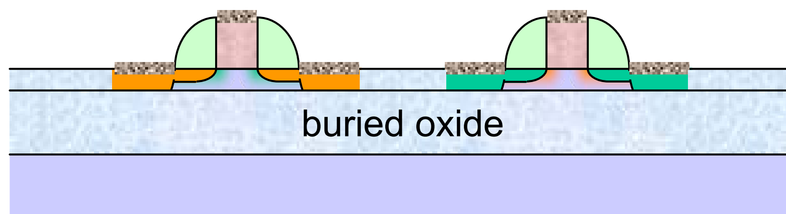
Accurate substrate modelling of RF CMOS

M. S. Alam[1,‡] and G. A. Armstrong[2,*,†]



MOSFETs with "no" substrates

fully-depleted (FD-SOI)



Alvin Loke, AMD

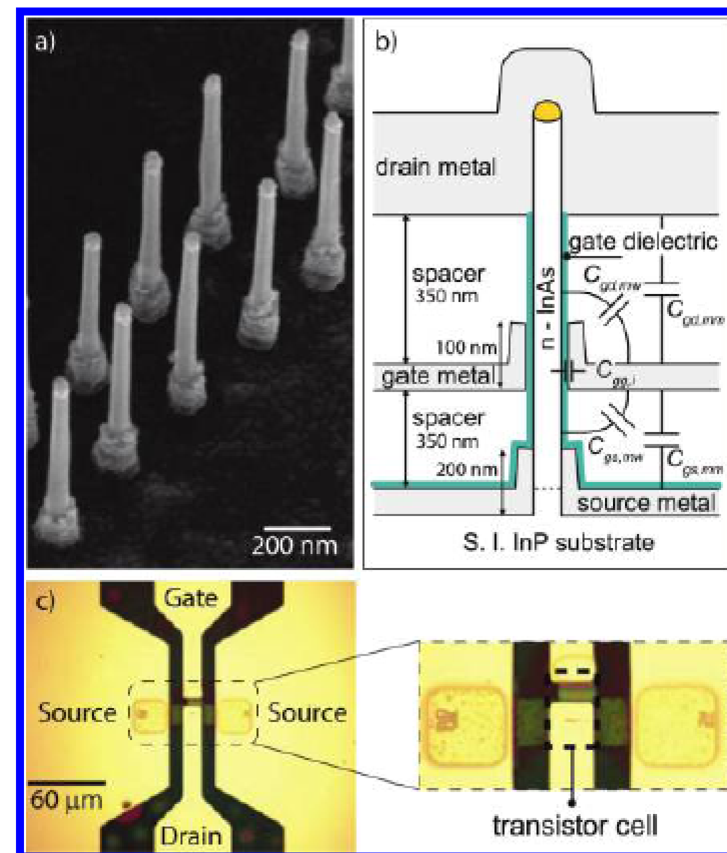


FIGURE 1. (a) Nanowire array with the bottom source ohmic contact, consisting of Al and W, wrapping around the NWs. (b) Schematic cross-section of the device, showing the thickness of the different layers and illustrating the device input capacitances. The gate length is about 100 nm. (c) Optical image of a completed device. The enlarged portion of the picture shows what is defined as the transistor cell.

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Vertical InAs Nanowire Wrap Gate Transistors with f_t > 7 GHz and f_{max} > 20 GHz

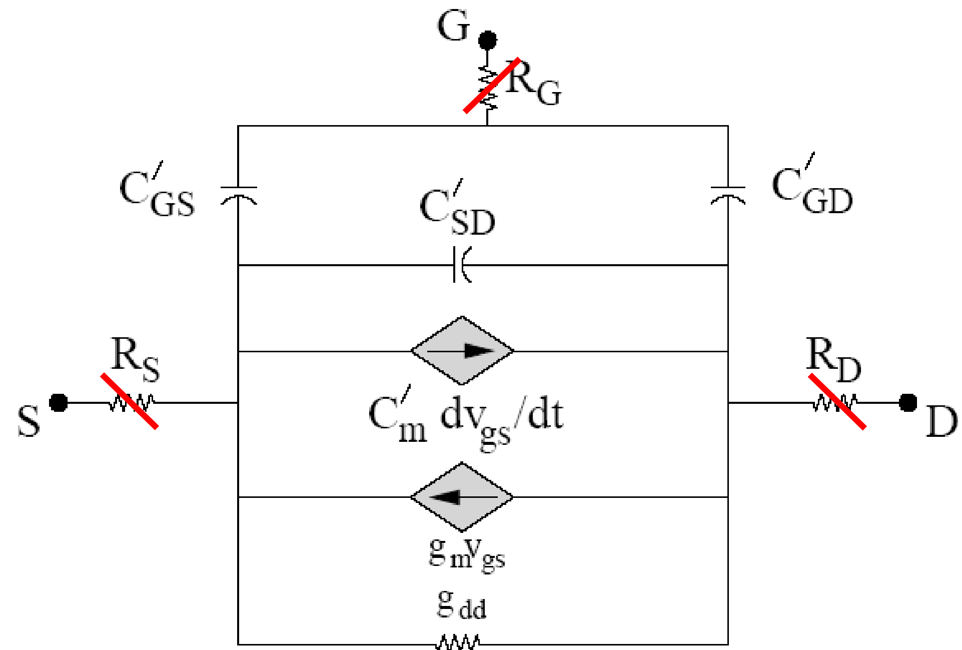
M. Egard,[*,†] S. Johansson,[†] A.-C. Johansson,[†] K.-M. Persson,[§] A. W. Dey,[§] B. M. Borg,[†] C. Thelander,[†,‡] L.-E. Wernersson,[§] and E. Lind[†,‡]

Nano Lett. **2010**, *10*, 809–812

Sec. 14.7.1

MOSFET intrinsic y-parameters

$$\begin{pmatrix} i_2 \\ i_3 \end{pmatrix} = \begin{pmatrix} y_{22} & y_{23} \\ y_{32} & y_{33} \end{pmatrix} \begin{pmatrix} v_{21} \\ v_{31} \end{pmatrix}$$



Remove R's

Rotate 90° to left

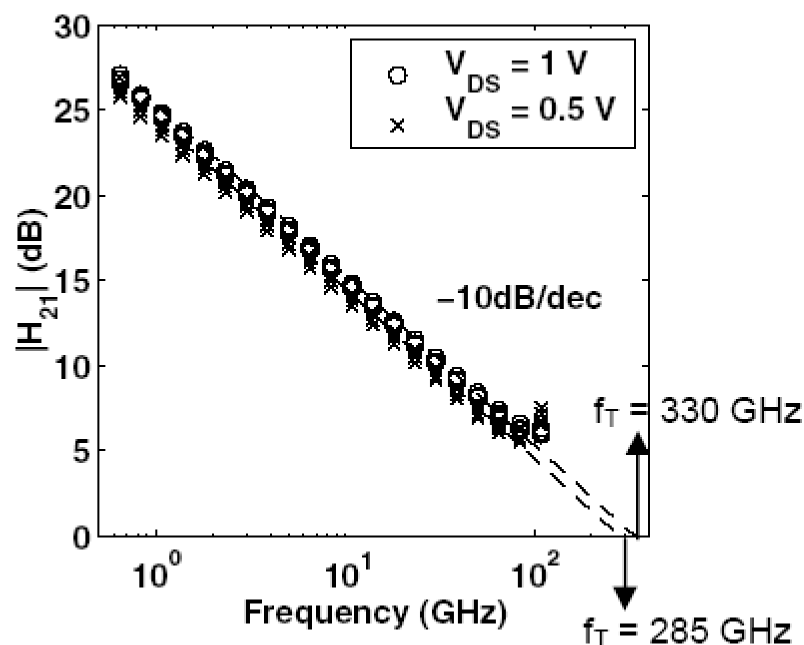
Shift G and D to the top

Relate y's to small-signal parameters

$$y_{22} = g_{dd} + j\omega(C_{sd} + C_{gd})$$
$$y_{23} = g_m - j\omega(C_m + C_{gd})$$
$$y_{32} = -j\omega C_{gd}$$
$$y_{33} = j\omega(C_{gs} + C_{gd}) \, ,$$

Intrinsic f_T from y-parameters

1. f_T is related to the short-circuit current gain
2. $|id/ig|^2 = |y23/y33|^2$
3. Extrapolated f_T is projection at -20dB/decade to gain = 1



IEDM Tech. Digest, 241-244, 2005

Record RF Performance of Sub-46 nm L_{gate} NFETs in Microprocessor SOI CMOS Technologies

Sungjae Lee*, Lawrence Wagner, Basanth Jagannathan, Sebastian Csutak, John Pekarik*, Noah Zamdmer, Matthew Breitwisch, Ravikumar Ramachandran, and Greg Freeman
IBM Systems and Technology Group, Hopewell Junction NY 12533,

Extrinsic z-parameters

1. Change INTRINSIC circuit to one using z-parameters
2. It's now easy to add in the parasitic R's
3. f_T is related to the short-circuit current gain
4. $|id/ig|^2 = |-z23/z33|^2$
5. Extrapolated f_T is projection at -20dB/decade to gain = 1

For an analytical expression, it's again necessary to selectively remove terms to get the required roll-off with frequency. the result is:

$$2\pi f_{\mathrm{T}} = \frac{g_m}{C_{gs}(1 + g_{dd}R_{sd}) + C_{gd}(1 + (g_m + g_{dd})R_{sd})}$$

Sec. 14.8

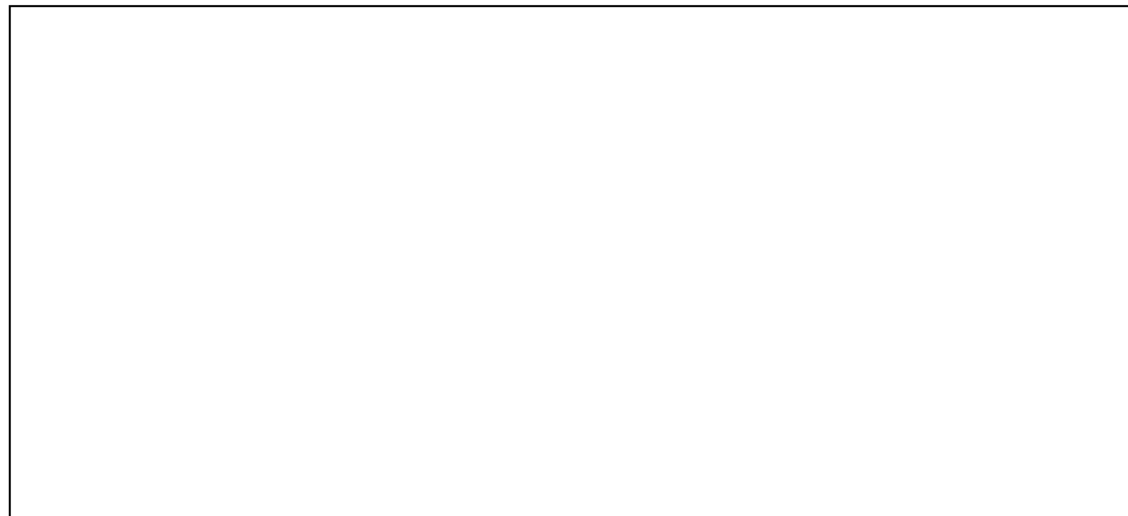
y- z- and s-parameters

y-parameters are measured from currents under various short-circuit conditions

z-parameters are measured from voltages under various open-circuit conditions

s-parameters are measured from powers under various matched conditions

s-parameter set-up



Why are s-parameters used in practice for HF measurements?

f_{max}

Another extrapolated frequency, this time referring to particular power gains.

We'll derive the one associated with MAG, the maximum available power gain.

Another one follows from U, Mason's Unilateral Power Gain, the expression for which is

$$U = \frac{|z_{23} - z_{32}|^2}{4[\Re(z_{33})\Re(z_{22}) - \Re(z_{32})\Re(z_{23})]}$$