Lecture 4

Power Distribution and Decap Design

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Overview

Reading

HJS - Chapter 11 Power Grid and Clock Design

Introduction

Power distribution used to be an afterthought in the design process before the issues of deep submicron brought in new challenges. Today, designers must be concerned with IR drop, Ldi/dt and electromigration while constructing the power system. The design process involves the selection of the overall architecture, placement of Vdd and Vss pins, design of the trunks, and ultimately the width of the wires. The power system is usually done hierarchically to manage complexity, but in the end the overall design must satisfy the noise budgets specified for the chip.

Decoupling capacitor (decap) design in deep submicron presents its own challenges and also affects the power grid design. This lecture highlights some of the key considerations in designing decaps suitable for high-speed applications.

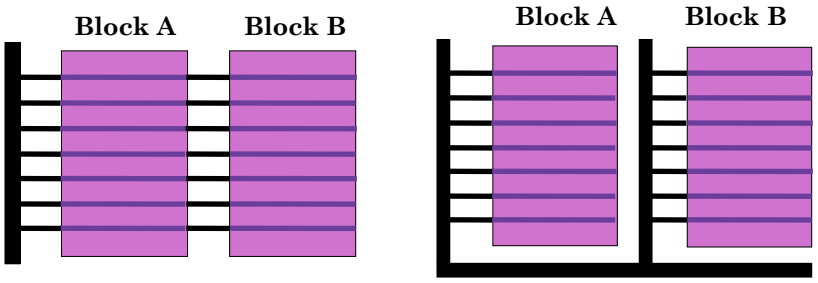
Purpose of Power Distribution

- Power distribution in the past was a fairly simple task
- Goal of power distribution system is to deliver the required current across the chip while maintaining the voltage levels necessary for proper operation of logic circuits
- Must route both power and ground to all gates
- Design Challenges:
  - How many power and ground pins should we allocate?
  - Which layers of metal should be used to route power/ground?
  - How wide should be make the wire to minimize voltage drops and reliability problems
  - How do we maintain V_{DD} and Gnd (i.e., Vss) within noise budget?
  - How do we verify overall power distribution system?

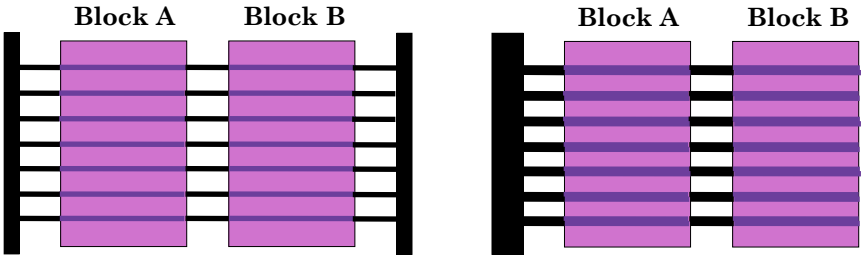
Importance of Power Distribution

- *Bad* power distribution: excessive voltage drop on the supply and/or excessive ground bounce due to IR drop and Ldi/dt effects.
- What problems can a bad power distribution cause?
  - Timing closure issues
  - Functional failure in extreme cases
- Power distribution has become a complex task in deep submicron
  - Thinner wires => increased wire resistance
  - More logic gates => higher current demand on chip
  - Higher operation frequency
- What if a power distribution problem that causes timing issues is identified at a late design stage (after placement & route)?

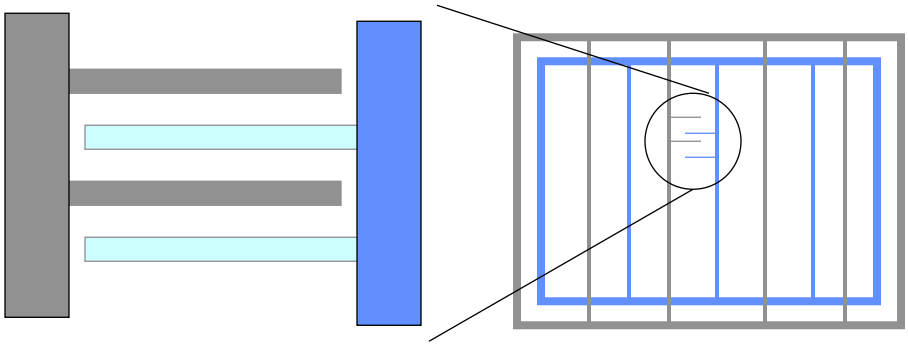
Power Routing Examples



Simple Routing Examples

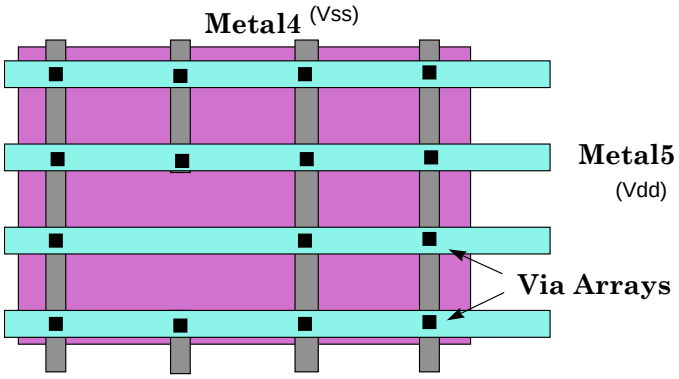


Interleaved Power/Ground Routing

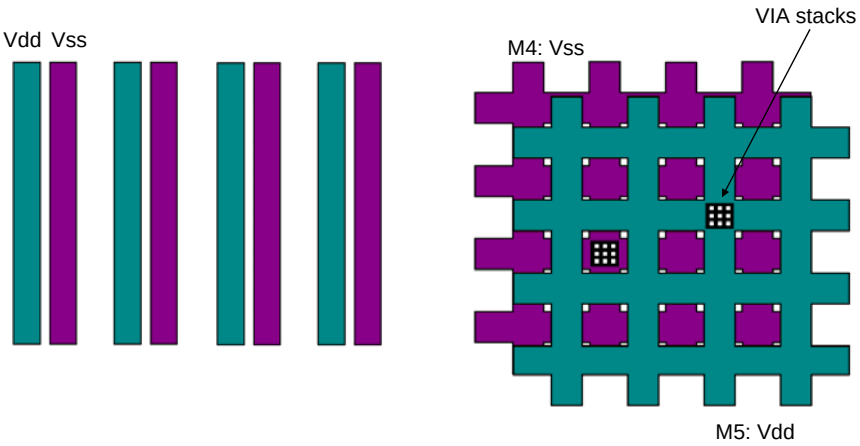


Interleaved Vdd/Vss pairs (e.g., standard cells)

Power Grid Architecture

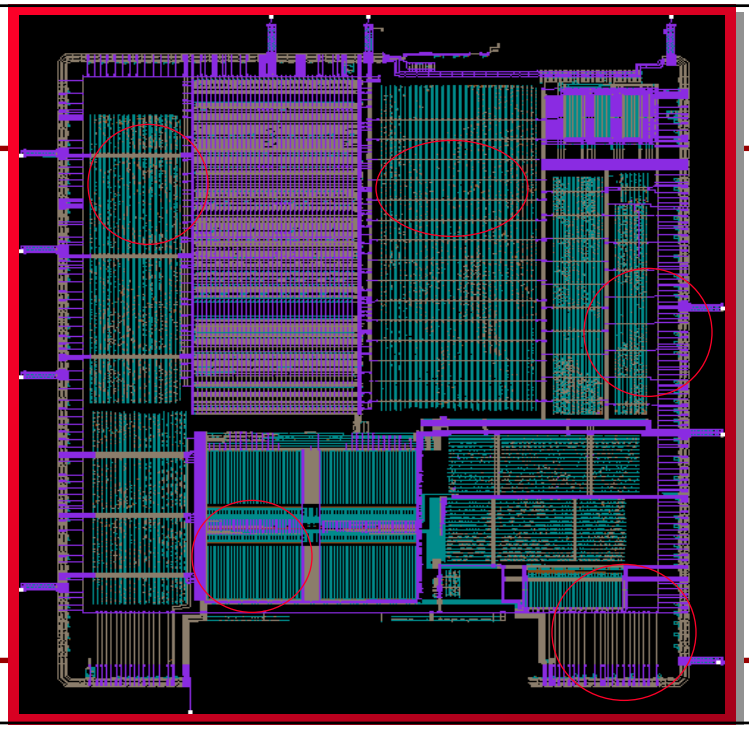


Other Popular Power Grid Architectures

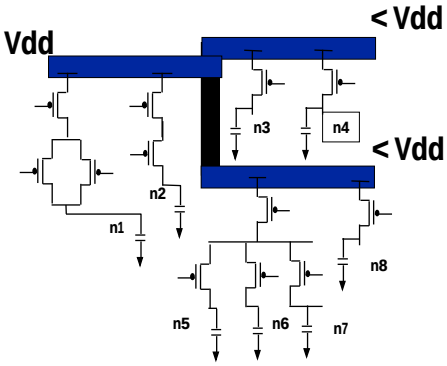


Single layer: straps

Dual layers: grid

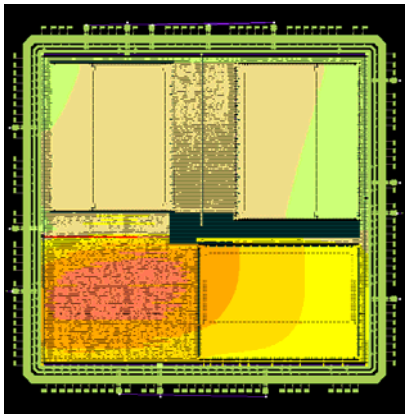


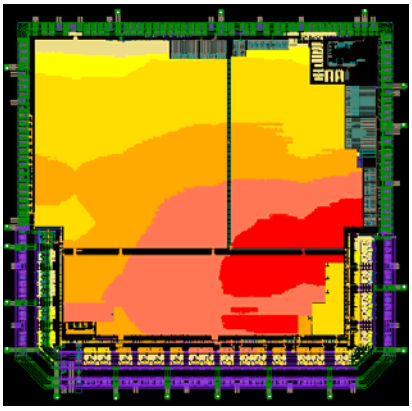
Power Distribution Issues - IR Drop



- Narrow line widths increase metal line resistance
- As current flows through power grid, voltage drops occur
- Actual voltage supplied to transistors is less than Vdd
- Impacts speed and functionality
- Need to choose wire widths to handle current demands of each segment

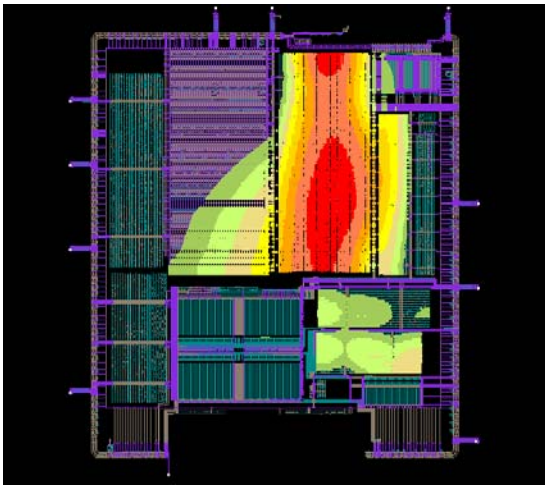
Block Interaction yields IR Drop





Plots courtesy of Simplex Solutions, Inc.

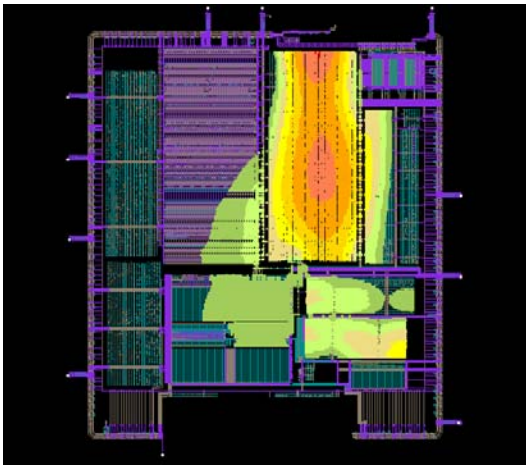
Power Grid Issues – Static IR Drop



- Block placement and global power routing determines IR drop on the chip
- Possible solutions
  - Rearrange blocks
  - More Vdd pins
  - Connect bottom portion of grid to top portion

Plot courtesy of Simplex Solutions, Inc.

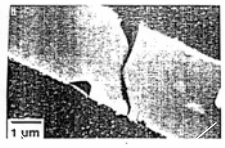
Power Grid Issues – Static IR Drop

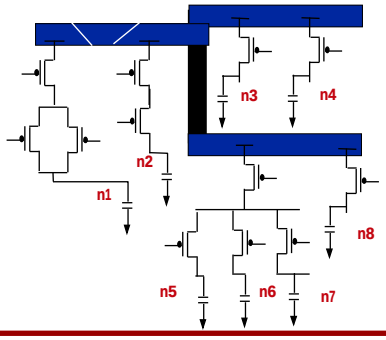


- If we connect bottom portion of grid to top portion, the IR drop is reduced significantly
- However, this is only one part of the problem
- We must also examine electromigration

Plot courtesy of Simplex Solutions, Inc.

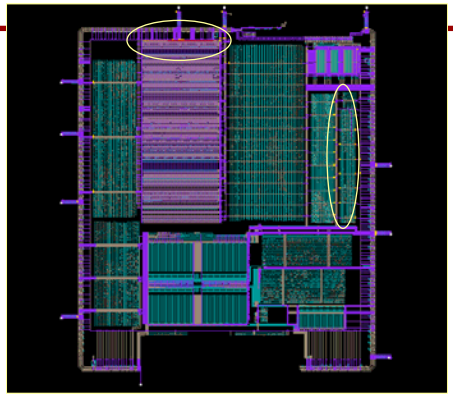
Power Grid Issues - Electromigration

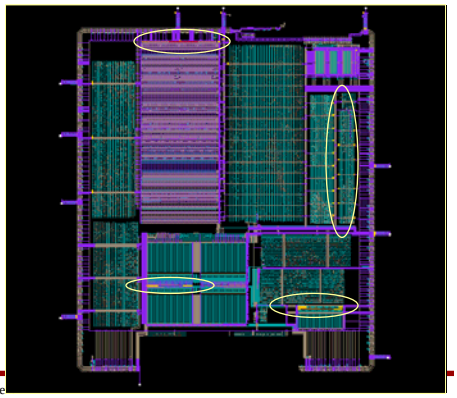




- As current flows down narrow wires, metal begins to migrate
- Metal lines break over time due to metal fatigue
- Based on average/peak current density
- MTTF -> Javg -> wire width
- Need to widen wires enough to avoid this phenomenon

Case Study – IR and EM Tradeoff





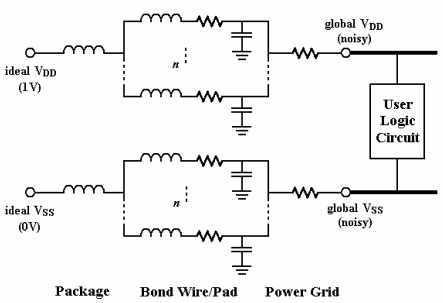
Simply connecting wires to remove IR drop violations may create more EM violations.

Ldi/dt Effects in the Power Supply

- In addition to IR drop, power system inductance is also an issue
- Inductance may be due to power pin, power bump or power grid
- Overall voltage drop is:

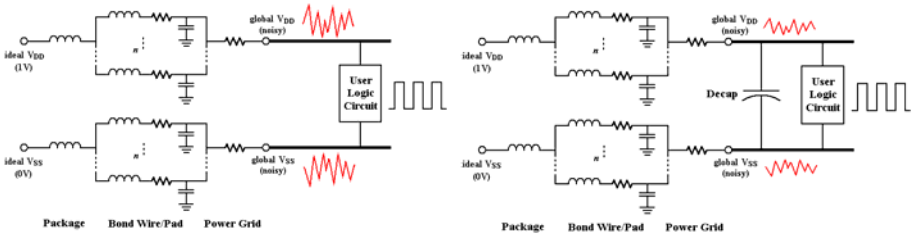
$$V_{drop} = IR + Ldi/dt$$

- A practical model for the power system:



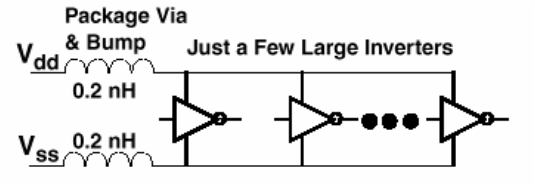
Decoupling Capacitors in the Power Supply

- Distribute decoupling capacitors (decaps) liberally throughout design
  - Capacitors store up charge
  - Can provide instantaneous source of current for switching



On-chip Decoupling Caps

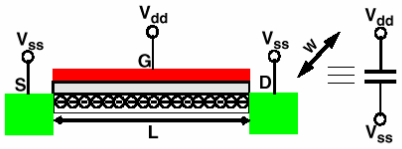
- On-chip decaps help to stabilize the power grid voltage
- First line of defense against noise which can extend beyond 10GHz
- Simple Example:



  - Drop across inductors = 2 x L x di/dt = 2 x 0.2nH x 20mA/100ps = 80mV (problematic if supply is 1V)
- Actual power pad or bump may need to support thousands of inverters
- Use capacitors to supply instantaneous charge to inverters

Making a Decoupling Capacitor

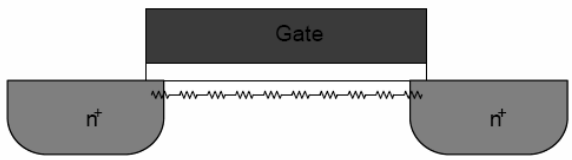
- Decaps are basically NMOS transistors. Top plate is polysilicon, bottom-plate is inverted channel, insulator is gate oxide.
- Connect poly to Vdd and source/drain to Vss



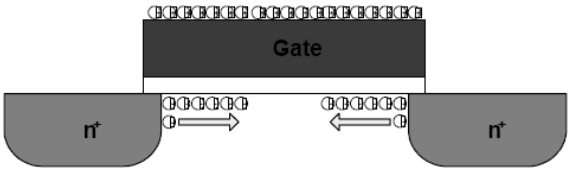
- Low-frequency capacitance is roughly C_{OX} W L.
- Since these are large capacitance to be used at high frequencies, more accurate representation is needed.

Decap High-Frequency Response

- Channel resistance in series with C_{decap} (affects response time)

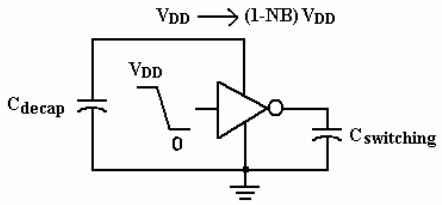


- Finite transit time (affects capacitance value)



How much Decoupling Cap?

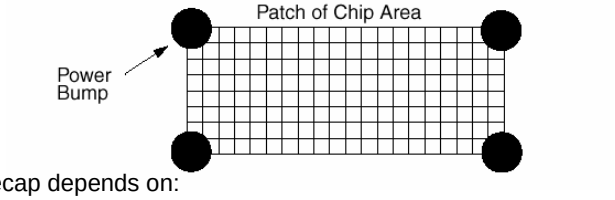
- For a rough calculation, consider the following example:



- Cdecap = Cswitching [(1-NB)/NB]
- For noise budget (NB) of 10%, Cdecap = 9 Cswitching
- Actual required decap is about 2~10X of the total on-chip switching capacitances. High-performance custom chips usually require more decaps.

How much Decoupling Cap?

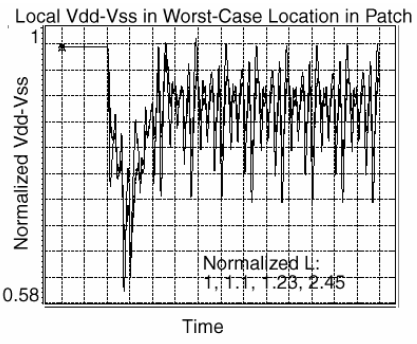
- To estimate required decap value, run SPICE on patch of chip area with power grid, part of logic block, and sprinkle of decaps



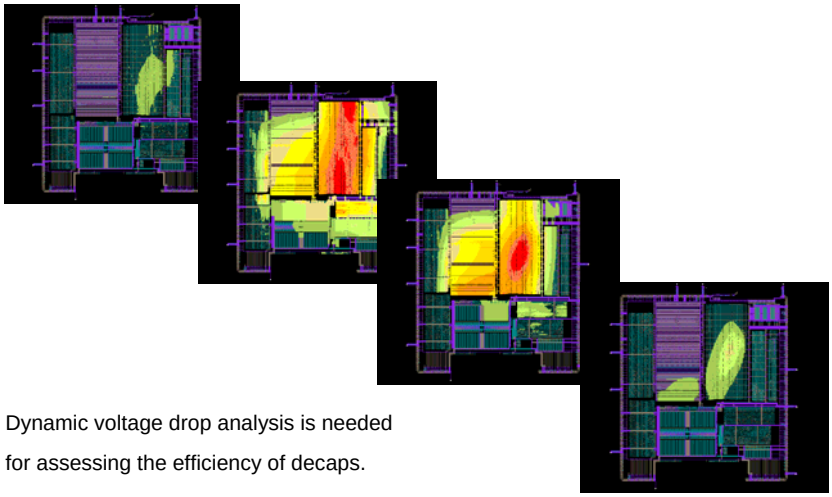
- Amount of decap depends on:
  - Acceptable ripple on Vdd-Vss (typically 10% noise budget)
  - Switching activity of logic circuits (usually need 10X switched cap)
  - Current provided by power grid (di/dt)
  - Required frequency response (high frequency operation)
  - How much parasitic decap exists (non-switching cap, gate, wire caps)

Simulation with Decoupling Caps

- Plot center region of grid
- Local Vdd-Vss in worst-case location in patch (center)
- First dip can be dealt with by a low-frequency on-chip voltage regulator and low-frequency decaps
- Steady-state ripple is controlled by high-frequency decoupling caps
- Adjust location of decaps until the ripple is within noise budget



Supply Noise is a Dynamic Phenomena



Dynamic voltage drop analysis is needed for assessing the efficiency of decaps.

Designing Power Distribution

- Floorplanner should be aware of IR+Ldi/dt drop and EM problems and design accordingly
  - Requires knowledge of current distributions and voltage drop constraints of blocks being placed
- Provide adequate number of V_{DD} and Gnd pins
- Route power distribution system according to current demands of the blocks
- Widen wires based on expected current density in branches
- Distribute decoupling capacitors liberally throughout design
- Verify full chip with IR/EM tools

Advanced Topics / Active Research Area

- Power gating
- Multiple voltage domains (voltage islands)
- On-chip voltage regulators
- Improving decap effectiveness
- Decap & logic codesign / IR drop aware floorplanning
- Optimal decap placement