EECE579 – Advanced Topics in VLSI Design

Assignment #1

(Due Wednesday, February 4, 2009)

Note: These problems are open-ended style problems so you can use any resources and ideas that you have to solve them. i.e., Use the class notes or textbook for any parameters that you need below. You will also need access to HSPICE in order to do the assignment.

1) FO4 Delay and Technology Trends (15 pts)

a) Assume a linear relationship between FO4 and L, as we showed in class. That is, let FO4 = $\tau \times L_{min}$. Using HSPICE, determine the FO4 delay for three different technologies (0.35 μm, 0.18 μm, and 0.13 μm). Draw a schematic of the circuit that you used and how you made your measurements. What is the coefficient, τ (in units of ps/μm) based on your simulation results? Explain any observations or assumptions that you have made to derive this value.

b) Based on this data, what is the FO4 delay for the 90nm and 65nm technology nodes. Does this match up with HSPICE results for these technologies? Assuming that 15*FO4 delays fit in one clock cycle, what are the clock speeds that derive from the FO4 results for these technologies?

c) Using fanout ratios in the range of 1 to 5, plot delay vs. fanout for 0.18um and 0.13um. What fanout gives the optimal delay in each case? What is your opinion about the trend of optimal fanout for delay as we scale to 90nm and 65nm?

2) Buffer Insertion (10 pts)

a) Wire delay increases quadratically with wire length. With proper repeater placement, the delay of a wire becomes linear with the length of wire. For a wire of length 40mm in a 90nm Cu technology, determine the optimal size of repeaters and number of segments. (hand calculations)

b) Compute the total delay through the buffered wire. For a 4GHz processor, how many flip-flops would be inserted in the wire to operate at this frequency? Draw a schematic of the resulting buffered wire with the flip-flops inserted.

3) Reading Assignments: (15pts)

Provide a 2-page summary of the following two papers (see website for PDF files):

a) R. Ho, et. al, "The future of wires"

b) R. Arunachalam, et. al, "Optimal shielding/spacing metrics for low power design"

Spend roughly 2 hours on each paper and then write the summary.