UNIVERSITY OF BRITISH COLUMBIA
Faculty of Applied Sciences
Department of Electrical and Computer Engineering

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EECE579
Spring 2006

Sample Midterm Questions

(open book, calculator permitted)

I hereby agree not to receive or provide help to any other student during this examination.

Signed_____ (sign name)

Problem 1	10pts	_____
Problem 2	15pts	_____
Problem 4	20pts	_____ (not covered in 2008 midterm)
Totals		_____
		(45pts)

Useful Parameters (90nm)	NMOS (Lmin=0.1um)	PMOS (Lmin=0.1um)
1X inverter	0.2um/0.1um	0.4um/0.1um
Req	12.5KΩ/	30KΩ/
Rsq (copper) = 0.054Ω/	N/A	N/A
Cg (gate cap per unit W)	2fF/um	2fF/um
Ceff (drain/source cap)	1fF/um	1fF/um
Cwire=0.2fF/um	N/A	N/A
Vdd=1V		

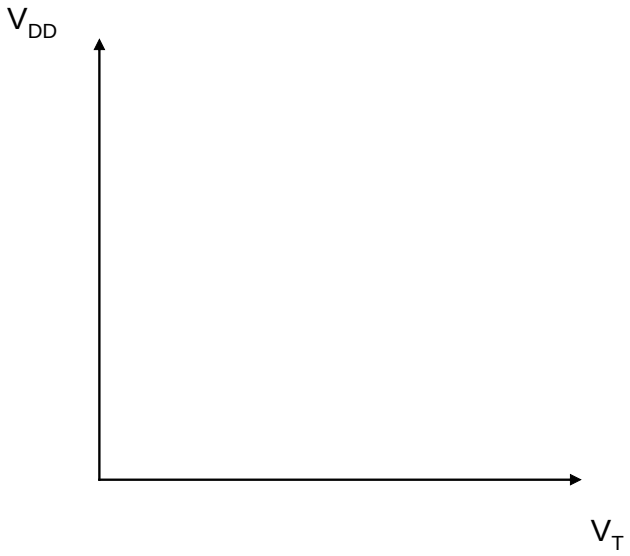
PRINT
NAME_____ STUDENT NO._____

1. Transistor Models and Scaling (10pts)

a) (4pts) Explain drain-induced barrier lowering (DIBL) using an NMOS device cross-sectional diagram. Why is it a concern today and what can be done to reduce its effect? Show this using a circuit diagram.

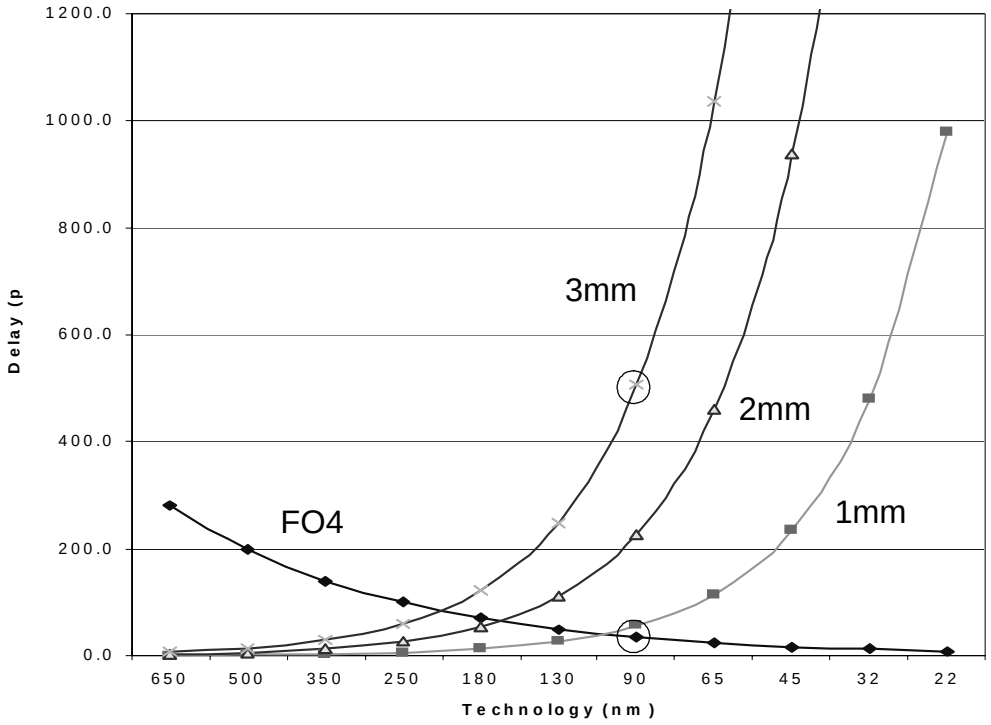
b) (2pts) As technology is scaling, V_{DD} is scaling faster than V_T. Explain why V_{DD} is scaling by a factor of 0.7 while V_T is scaling by 0.9, and the associated tradeoffs. What are process engineers doing to help designers?

c) (4 pts) Write the equations for dynamic power and static power (separately). In the plot of V_{DD} vs. V_T, sketch the contour lines of constant dynamic power and constant static (subthreshold leakage) power. (note: calculations are not required)



2. Wires and Wire Models (15 pts.)

a) (8pts) The graph shown below shows the FO4 delay of a gate and the delay of three different wire lengths as a function of technology scaling. Show how you would obtain the circled values. That is, show the details of how you would compute the FO4 delay, and then the wire delay for a 3mm wire in a 90nm technology node. What assumption do you have to make about the wire width? Is this a reasonable assumption?



(continue with solution on this page)

b) (7pts) A clock cycle of 10 FO4 delays is used for a processor design in a 90nm copper technology. However, the chip is so large that it is impossible to get a global signal across the chip in a single clock cycle.

   i. (1pt) Estimate the maximum possible wire length that one can have in the design, assuming that it is unbuffered, based on the graph on the previous page?

ii. (6pts) Estimate how long a wire can be, assuming that it is buffered, before we have to insert a flip-flop in the signal path? That is, what is the maximum buffered wire length possible? (hint: take a long wire, perform buffer insertion, determine the delay of each section, and finally how many sections fit into a 10FO4 clock cycle)

3. Various Topics in SoC/DSM (20 pts)

a) (2pts) When designing a reusable IP block, what portion of the design cycle takes the longest to complete? For a platform-based design, what is the most time-consuming portion?

b) (2pts) Why is the MIPS processor more popular than the ARM processor in the set-top box application?

c) (4pts) List 4 major issues that are expected at the 65nm technology node.

d) (2pts) Which is the bigger concern today in power supply noise, IR drop or Ldi/dt variations? Why?

e) (3pts) What is the typical cost of a mask set at 90nm? What is the overall design cost for a 50M transistor chip? In that case, why are designers so worried about mask costs?

f) (4pts) Briefly describe scan-based testing using a diagram. Why is scan-based testing such a popular technique in the industry? What are the limitations and overhead associated with the approach.

g) (3pts) In a two-column format, compare and contrast EEPROMs with FLASH memories.