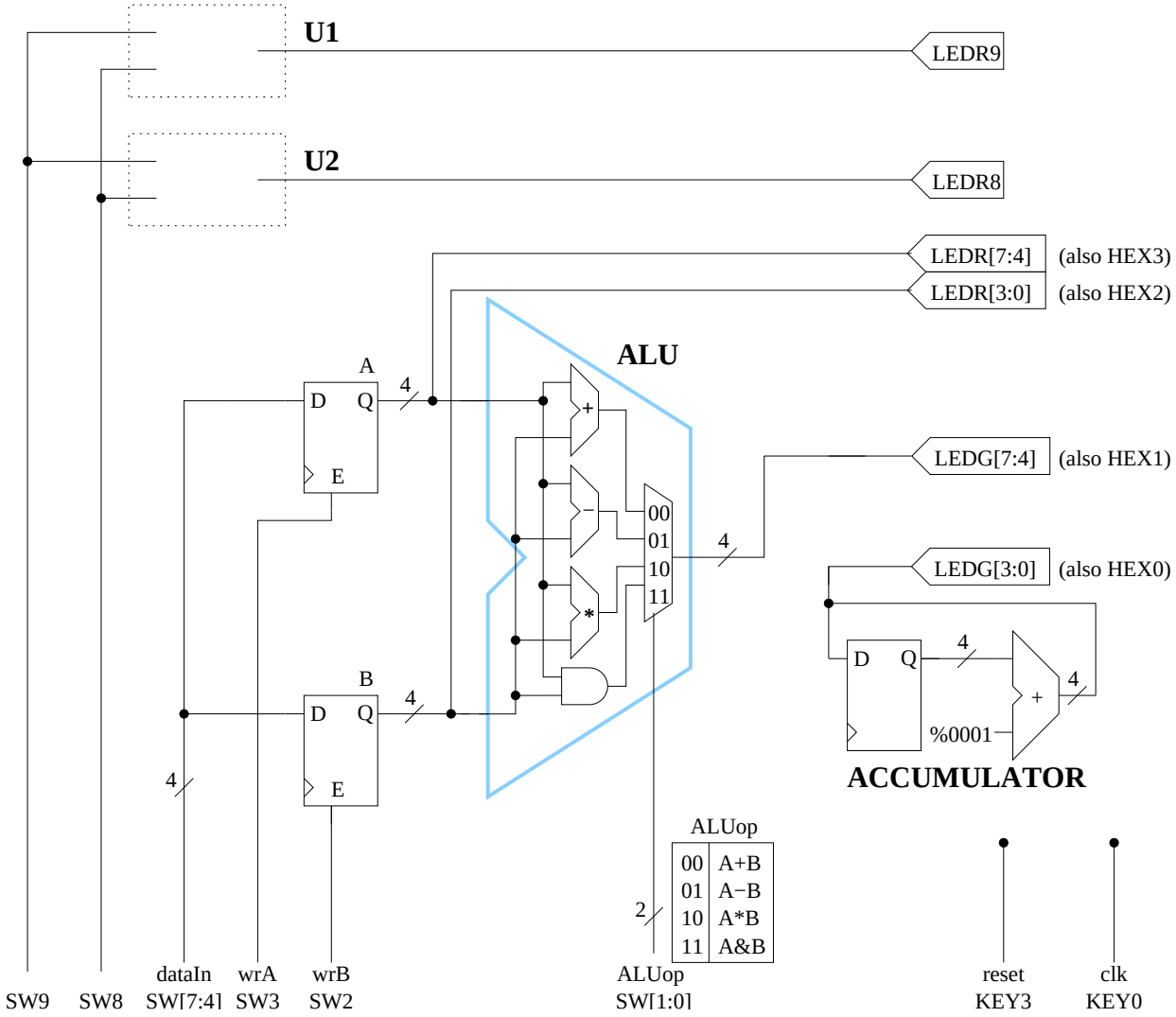

Figure A. Basic Logic Gates circuit.

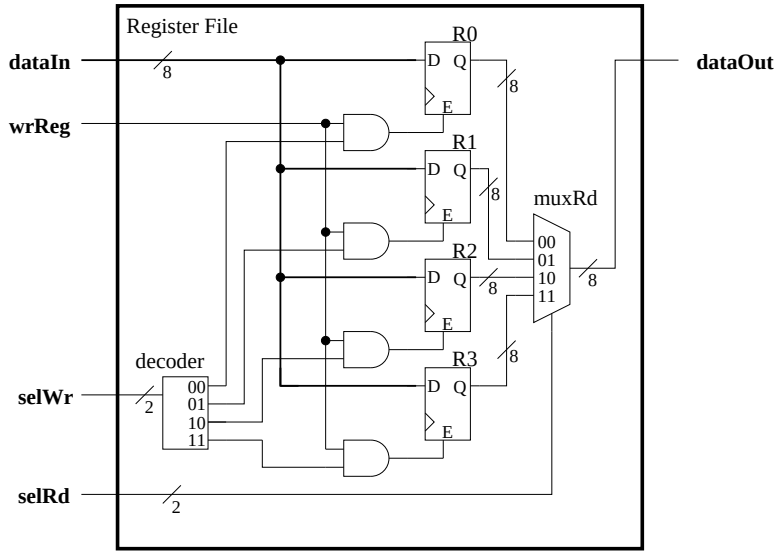

Figure B1. Register File details.

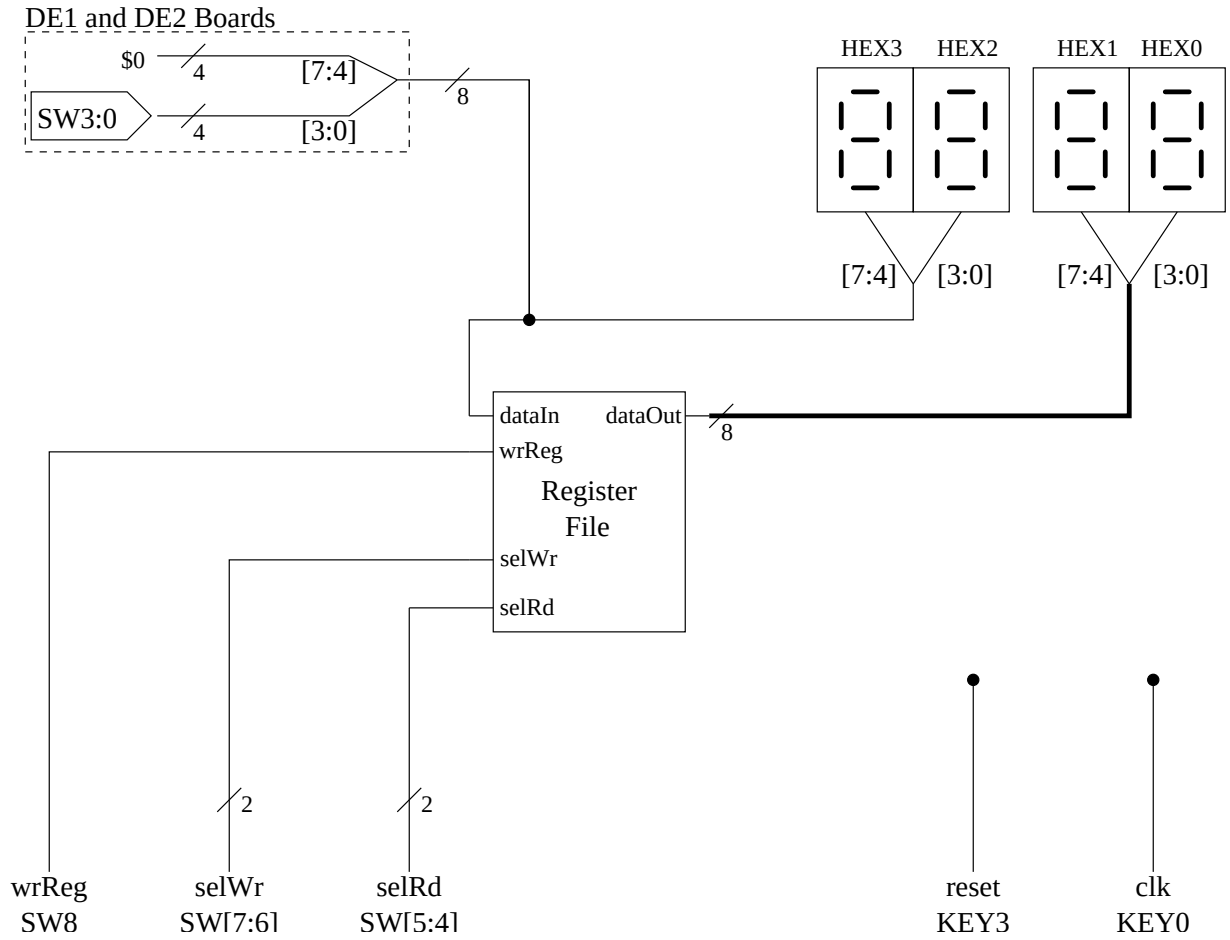

Figure B2. Register File circuit.

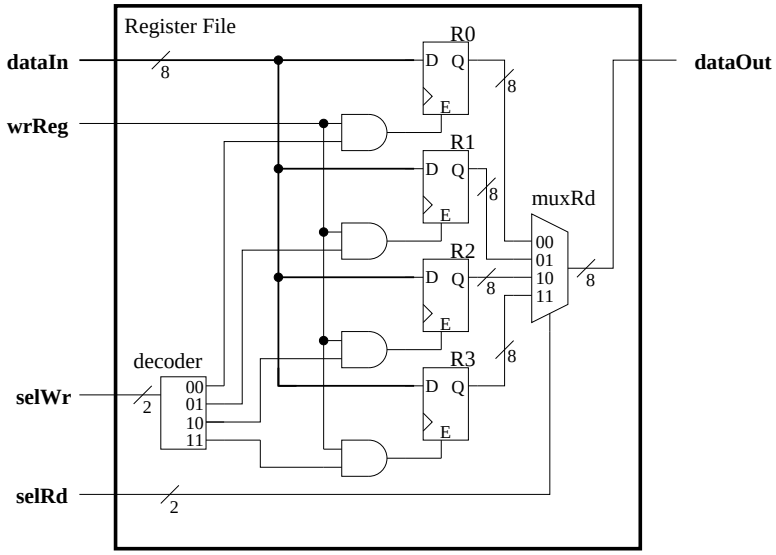

Figure C1. Register File details (same as Figure B1).

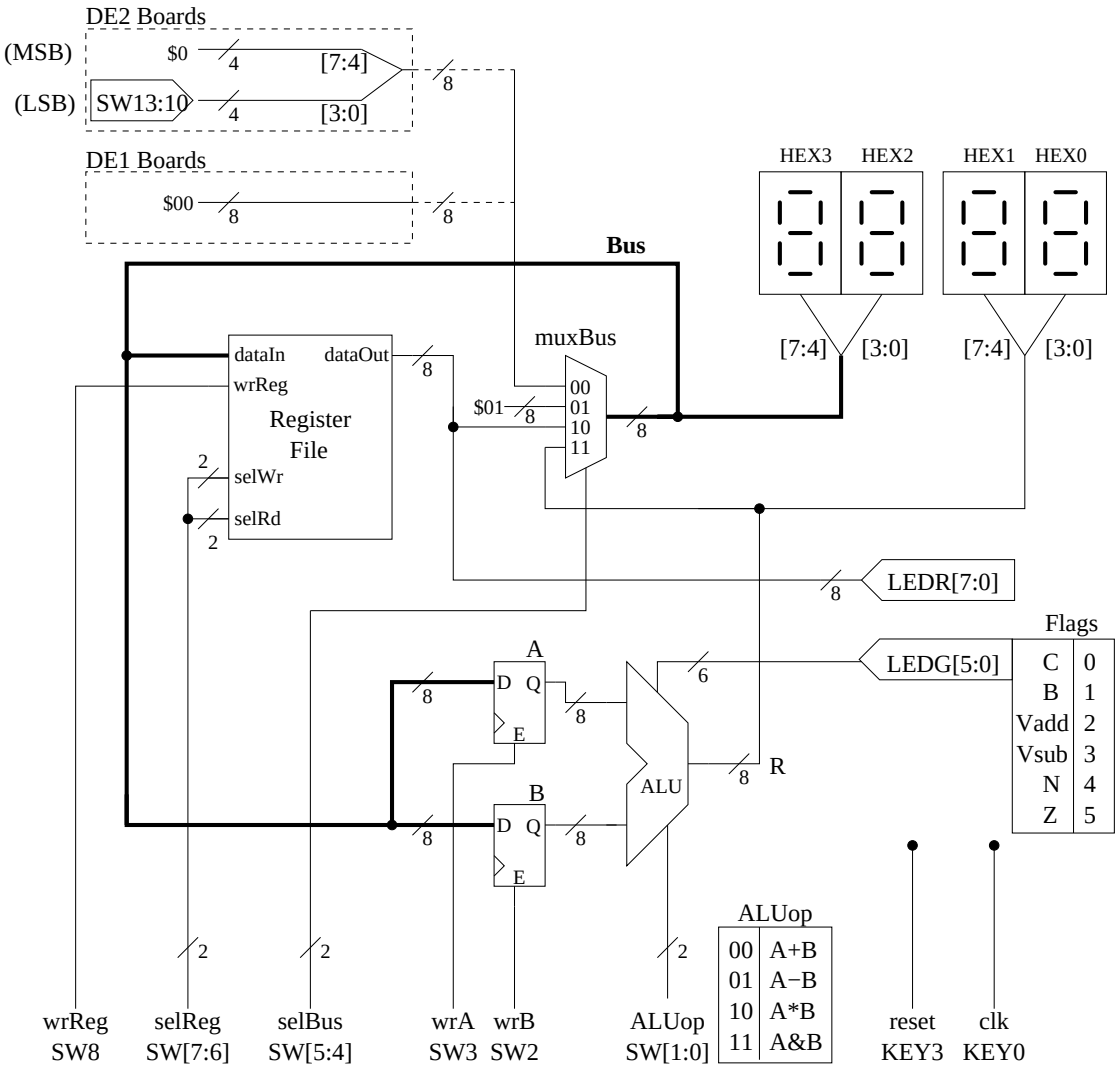

Figure C2. Computational Datapath circuit.