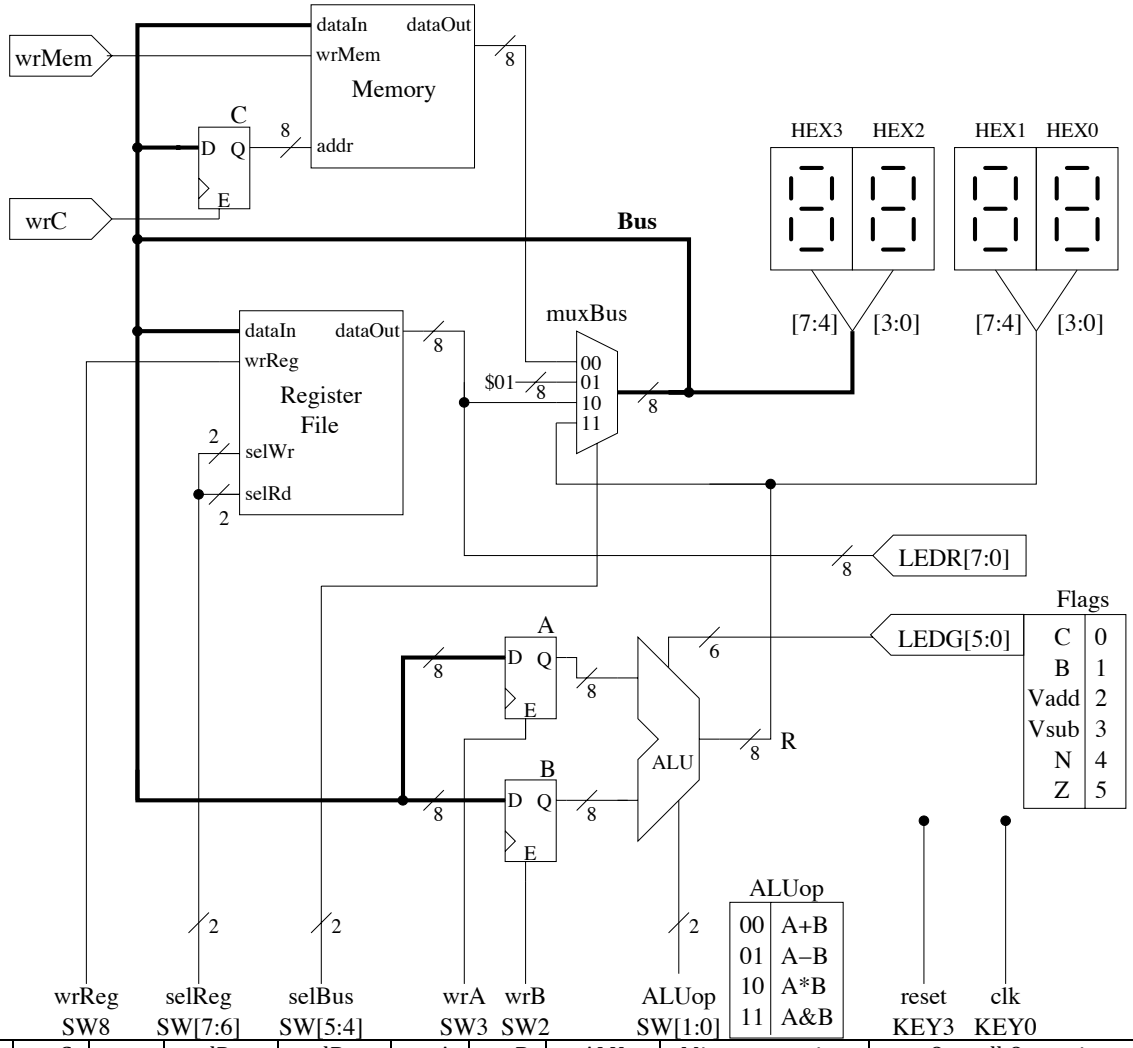

Cycle #	wr Mem	wrC	wr Reg	selReg [1:0]	selBus [1:0]	wrA	wrB	ALU op[1:0]	Micro-operation	Overall Operation
1										
2										
3										
4										
5										
6										
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