THE UNIVERSITY OF BRITISH COLUMBIA
Department of Electrical and Computer Engineering

ELEC 391 – Electrical Engineering Design Studio II

Lab Assignment 3 – Phase-Locked Loops

1 Introduction

This lab assignment is concerned with practical issues associated with the implementation of phase-locked loops. In particular, we focus on the CMOS 4046 Phase-Locked Loop.

The test and measurement equipment (and measurement accessories) used here include a function generator, oscilloscope, DC power supply, and breadboard.

We place particular emphasis on accurate and honest comparison between theoretical predictions (or manufacturer's design formulas) and experimental results. Where discrepancies exist, possible and realistic explanations should be offered.

1.1 Performance Objectives

Upon completion of this lab assignment, ELEC 391 students will be able to:

- Explain the function and operation of phase-locked loops using simple mathematical models.
- Design, implement, and evaluate the performance of phase-locked loops using standard components, test and measurement equipment, and measurement accessories.

1.2 Tasks

Completing this lab assignment will involve the following steps:

1. *Before your first assigned lab period:* Review the lab assignment and begin the prelab assignment in Section 2 on your own! Although the assignment will not be formally marked, it will be checked for completeness and correctness and will be considered when your mark for this lab assignment is assigned.

   Meet with your lab partners to discuss the lab assignment and to assign responsibilities during the lab session.
2. *During the scheduled lab period:* Submit your individual prelab assignment for informal review and work with your lab partners to complete the three experiments described in the lab assignment handout.
3. *During the few days after your first assigned lab period:* Meet with your lab partners to plot and/or reduce your data, to draw conclusions, and to the group lab report.
4. *Three days after your second assigned lab period:* Submit your group lab report for marking.

1.3 Test and Measurement Equipment

The following test and measurement equipment will be used in this lab session. Copies of the equipment manuals will be available in the lab. Where applicable, please record the serial number of each item.

1. Function/Arbitrary Waveform Generator (Rigol, model DG1022, 2 Channel, 20 MHz, 100 MSa/s)
2. Dual-channel oscilloscope (Tektronix, model TDS 2012C, 100 MHz)
3. Power supply

We supply the components, but you are expected to supply your own breadboard and hand tools.

2 Prelab Assignment

Before you come to the lab, please review both (1) the CD4046BC data sheet from Fairchild and (2) this entire lab assignment in detail. Then complete the following tasks:

1. Using the manufacturer's design curves, select C_1, R_1, and R_2 so that the VCO operates from f_{min} = 8 kHz to f_{max} = 12 kHz. Find the VCO frequency sensitivity K_0 assuming that the VCO characteristic $f_{osc}(v_c)$ is linear from $0 < v_c < V_{DD}$. The supply voltage is V_{DD} = 15 V.
2. Select values of C_f and R_f that will yield a low-pass filter with cut-off frequency f_p = 1 kHz.
3. Select a value of C_i appropriate for input signals with frequencies in the 5 kHz to 15 kHz range.
4. Assume that $v_i(t)$ is a square-wave signal with frequency f_i, that the PLL is in the locked condition ($f_{osc} = f_i$), and that v_o is a dc voltage with negligible ac component. Sketch and label $v_i(t)$ and $v_{osc}(t)$, and determine the voltage v_c for:
   a. f_i = 9 kHz,
   b. f_i = 10 kHz,
   c. f_i = 11 kHz.

3 Experiment 1: Characterization of the Voltage Controlled Oscillator

3.1 Objectives

The objectives of this experiment are: (1) to develop empirical design formulas for the VCO minimum and maximum frequencies and (2) to determine the VCO transfer function $f_{osc}(v_o)$.

3.2 Procedure

1. The design formulas for the VCO minimum frequency f_{min} and maximum frequency f_{max} that are given in the 4046 data sheet are only approximate. Experimentally determine R_1, R_2, and C_1 so that f_{min} = 8 kHz and f_{max} = 12 kHz. Note that the VCO will generate f_{min} when pin 9 in pulled to ground and f_{max} when pin 9 is pulled to V_{DD}.
2. Measure and plot the VCO transfer characteristic $f_{osc}(v_c)$ for $0 < v_c < V_{DD}$. Do not connect the loop filter.

3.3 Issues for Discussion

1. Express the results of Step 1 in the form of design formulas for the maximum and minimum frequency. The design formulas should be of the form

$$f_{min} = \frac{k_1}{R_2(C_1 + 32\text{ pF})},$$

and

$$f_{max} = f_{min} + \frac{k_2}{R_1(C_1 + 32\text{ pF})}.$$

2. In the range $(v_c)_{min} < v_c < V_{DD}$, the VCO output frequency should be a linear function of v_c. For $v_c < (v_c)_{min}$, the frequency does not depend upon v_c. Determine
   a. $(v_c)_{min}$,
   b. the free-running VCO frequency for $f_0 = V_{DD}/2$, and,
   c. the gain K_o of the VCO.
3. If the VCO characteristic is linear, K_o can be determined from the end-points of the linear range,

$$K_o = \frac{f_{max} - f_{min}}{V_{DD} - (v_c)_{min}}.$$

   The slope of a straight-line interpolation through the measured points for $v_c > (v_c)_{min}$ should give the same result. Comment on the trade-offs between the two approaches.

4 Experiment 2: Operation of a Phase-Locked Loop

4.1 Objective

The objective of this experiment is to characterize the operation of the phase-locked loop with the loop closed, *i.e.*, with the RC loop filter inserted between the phase detector output and the VCO input.

4.2 Procedure

1. Use a function generator to generate a square wave with amplitude of approximately 1 $V_{p\text{-}p}$ and frequency f_i that approximately matches the free-running frequency f_o of the VCO.
2. When v_i is applied, the PLL should operate in the locked condition with f_{osc} exactly equal to f_i. Verify this by observing both the input and output signals *simultaneously* using a dual-trace oscilloscope, both before and after the input signal is applied to the output of the phase detector.
3. Vary f_i of the input signal in order to determine the *lock range* of the PLL. That is, determine the maximum and minimum frequencies to which the input signal can be set while the PLL output signal continues to track the input signal.
4. Determine the minimum peak-to-peak amplitude of the input signal v_i such that the PLL remains locked.
5. Sketch the waveforms v_i, v_{osc}, and v_ϕ for the PLL in the locked condition when the frequency of the input signal is set to the free-running frequency, the lowest frequency in the lock range and the highest frequency in the lock range.
6. Measure and sketch the characteristic $v_c(f_i)$ of the PLL. Since f_{osc} is directly determined by v_o, this characteristic should have the same form as the characteristic $f_{osc}(f_i)$ given in the lecture. Because the transfer characteristic exhibits hysteresis, it will be necessary to vary f_i in both directions in order to completely characterize the curve.

4.2 Issues for Discussion

1. Explain the criteria that you used to verify that f_{osc} was exactly equal to f_i in Step 2.
2. Compare the lock range and minimum signal determined in Steps 3 and 4 with the values predicted by the manufacturer.
3. Compare the phase difference ϕ between v_i and v_{osc} to the theoretical prediction for the three frequencies in Step 5.
4. Compare the characteristic $v_c(f_i)$ to the curve given in the lecture.

5 Experiment 3: Effects of Changing the Loop Filter

5.1 Objective

The objective of this experiment is to determine the manner in which changing the cut-off frequency f_p of the loop filter affects: (1) the capture range of the PLL and (2) the high frequency ripple in v_o.

5.2 Procedure

1. Select appropriate values of R_f and C_f that will yield instances of the loop filter that will cover the range 100 Hz < f_p < 10 kHz.
2. Measure and plot, as functions of f_p,
    a. the end points of the capture range, and the capture range $2f_c$, and,
    b. the peak-to-peak ac ripple on the filter output voltage v_o,
        i. when the PLL is locked, and,
        ii. when $f_i = f_0$.

5.3 Issues for Discussion

Compare the measured results with theoretical predictions and/or manufacturer's design formulas. Comment upon and suggest possible explanations for any discrepancies that were observed.