THE UNIVERSITY OF BRITISH COLUMBIA
Department of Electrical and Computer Engineering

ELEC 391 – Electrical Engineering Design Studio II

Phase-Locked Loops – Review Questions

The purpose of this short self-quiz is to help you review the essential parts of the lectures on *Phase-Locked Loops*. Most of the answers can be found in the lecture notes.

SQ3R – Survey, Question, Read, Recite, Review

Introduction

1. What is a phase-locked loop?
2. When was the phase lock principle first reported?
3. What was the first widespread application of PLL technology?
4. Why did NASA begin using PLL's in the early 1960's?
5. What effect has integrated circuit technology had on PLL applications?
6. What are typical applications of PLLs?

1. Basic Architecture of a Phase-Locked Loop

1.1. Sketch a phase-locked loop and: (1) identify its major functional blocks and (2) label the signals that appear at the output of each functional block.

1.2. What is the purpose of the phase detector?

1.3. What is the purpose of the loop filter?

1.4. What is the purpose of the voltage-controlled oscillator (VCO)?

1.5. What is the purpose of the divider?

1.6. If the input frequency and the VCO output frequency are sufficiently close to each other, what will the PLL do?

1.7. What is the capture range of a PLL?

1.8. What is the lock range of a PLL?

2. Applications of Phase-Locked Loops

Frequency Synthesis

2.1. What is the principal limitation of a free-running oscillator that prevents its widespread use in RF transmitters?

2.2. What are the principal strengths and limitations of a crystal-controlled oscillator when used in RF transmitters?

2.3. Sketch and label a PLL-based frequency synthesizer.

2.4. How does a PLL-based frequency synthesizer overcome the limitations of crystal-controlled oscillators?

2.5. What is the principal limitation of a PLL-based frequency synthesizer?

2.6. What sets the frequency range, frequency resolution and output frequency of a PLL-based frequency synthesizer?

2.7. What is the purpose of the prescaler?

FM Demodulation

2.8. How do filter-based FM demodulators function? What is their major limitation?

2.9. Sketch and label a PLL-based FM demodulator.

2.10. Explain how a PLL-based FM demodulator functions.

Motor Speed Control

2.11. Explain how a DC motor equipped with an optical shaft encoder functions like a VCO.

2.12. Sketch and label a PLL-based motor speed controller.

2.13. Explain how a PLL-based motor speed controller functions.

2.14. What are two common applications of PLL-based motor speed controllers?

3. Issues in Phase-Locked Loop Design

3.1. What are the three principal issues in phase-locked loop design?

4. Implementation of a Phase-Locked Loop

4.1. On what integrated circuit technology is the 4046 PLL based?

4.2. How is the value of the input capacitor selected?

Phase Detector

4.3. What types of phase detectors are implemented on board the 4046 PLL?

4.4. What is the principal advantage of the XOR-based phase detector?

4.5. What is the nature of the signal that appears at the output of the XOR gate?

4.6. Using a timing diagram, explain how one can use an XOR-based phase detector to measure the phase between two signals.

4.7. What restrictions are placed on the signals that one applies to an XOR-based phase detector?

4.8. Sketch and label the transfer function of an XOR-based phase detector.

Loop Filter

4.9. How is the loop filter in a 4046-based PLL implemented? What is its order?

Voltage Controlled Oscillator

4.10. When does the VCO aboard the 4046 PLL deliver its minimum and maximum frequency?

4.11. How does one set the value of the minimum and maximum frequency of the VCO?

Operation of the 4046 Phase-Locked Loop

4.12. What is the output of a PLL when no input signal is present?

4.13. What causes the output frequency of a PLL to begin tracking the frequency of an input signal?

4.14. Why is there a phase difference between the input and output signal when the PLL is locked?

Lock and Capture Ranges

4.15. What determines the lock and capture ranges of a PLL?

4.16. What tradeoffs must be considered when setting the capture range of a PLL?