EXTRACTS FROM

EECS 142 Laboratory #1

High Frequency Passive Components

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1 Introduction

Passive components play an important role in RF and microwave circuits. For instance, inductors are commonly employed to tune out the capacitance of transistors by forming resonant circuits. Inductors and capacitors together are used to build filters and impedance matching circuits. In communication circuits, filtering and matching are important functions for attenuating unwanted signals while maximizing the gain of desired frequencies. Unfortunately, there are no ideal inductors, capacitors, or resistors, and the unwanted characteristics of these components are called parasitics. In this laboratory, you will learn about the high frequency parasitics associated with passive components. These parasitics add loss and limit the upper frequency range over which the components function properly.

2 PCB Manufacturing

All circuits will be fabricated using a simple two-layer printed circuit board (PCB). The PCB consists of a low-cost dielectric material, usually FR4 ($\epsilon_r = 4.4$), with a thickness of 62 mils[1], and two layers of Cu metal layer. The copper layers are plated with solder, which doesn't oxidize and which melts at low temperature. The metal layers have a thickness of 34 μm. Normally you would pattern the metal layers to produce your circuit but in the interest of time, the boards have been prefabricated to take on a standard form. The backside of the board is a solid ground plane. Connections to ground must travel through a plated-through "via" to reach the backside.

A typical board used in later labs shown in Fig. 1. The input and output of the board have footprints for SMA connectors which allow you to connect SMA cables[2]. The input and output microstrip transmission lines are interrupted periodically which allow you to place components in series or in shunt. Landing pads with vias to ground also appear periodically to allow shunt components to be soldered to ground.

To solder components onto the board, use standard 0603 components[3] in series or in shunt. The components have lead-free solder plating (as all do, these days), so use lead-free solder. Also, use flux which is formulated specifically for lead-free soldering. See the ppt file on the class website for tips on precision soldering of 0603 lead-free components.

While Fig. 1 shows the amplifier board you'll use in Lab 3, the actual boards you'll be using in this lab are shown in Fig. 19 and Fig. 20. We'll make the assumption that the parasitics we characterize on the test boards in this lab, will be the same for the boards in, say, Lab 3. While this won't be completely true (FR4 material is low-cost with a large thickness tolerance so all boards might not have the same thickness). Nevertheless, we will make the assumption that however you characterize the parasitics in this lab, you can use those parasitic models for the boards used in later labs.

Another assumption we'll make is that the connectors' behavior is reproducible. The

[1] 1 mil = .001 inch = 25.4 μm

[2] SMA stands for SubMiniature version A, a connector for coaxial cables with 50Ω impedance and good performance up to 18GHz

[3] Components are classified according to their footprint size in mils, or in this case 0.060 inches by 0.030 inches.

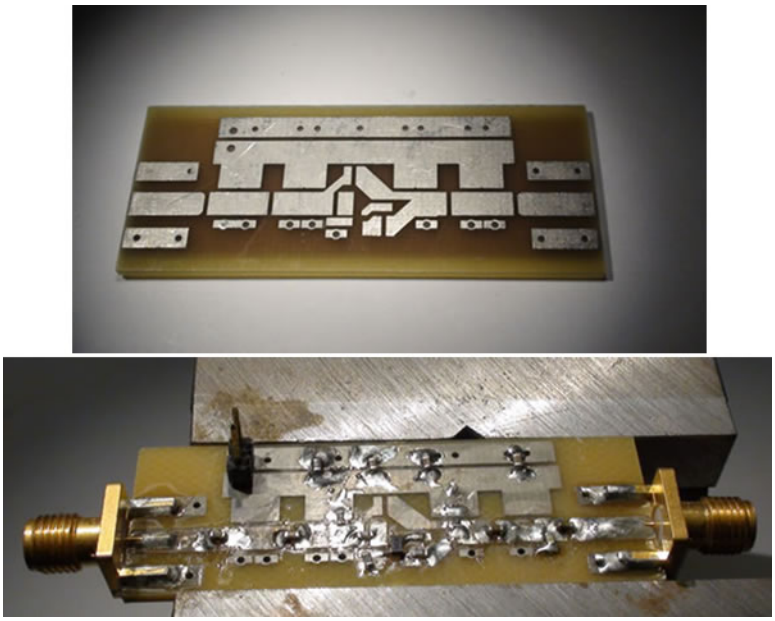

Figure 1: Top) Bare amplifier board to be used in Lab 3. Bottom) Stuffed version of the above board implementing a tuned amplifier for narrowband operation at 600 MHz. The point of this Lab 1 is to characterize the parasitics of these boards: the microstrip transmission lines (seen most clearly in the upper photo), and the gaps between transmission lines where you will solder components. You'll also characterize the intrinsic parasites of the 0603 components themselves. Whenever you use such components in later designs, you'll need to account for both the 0603's intrinsic parasitics and the 0603's extrinsic parasitics which arise from how it's mounted onto the board - so that you can design high-frequency circuits in later labs that will work correctly as designed

term "repeatable" is used to mean the behavior is the same when we connect and remove one connector from the same mating connector. The term "reproducible" is used to mean that the SMA connectors you have on your Lab 1 boards will behave the same as the SMA connectors on your Lab 3 board. Connectors have tolerances also, so they can't behave identically, but we'll assume they do. Just be aware of what assumptions are buried in these labs.

One thing we won't assume, is that the designer of these boards was successful in creating 50 ohm transmission lines. It's always possible that a panel gets over-etched or under-etched, so that the traces come out wider or skinnier than the designer specified. You'll characterize the transmission line of a "Thru" board in this Lab 1 (on a per-length basis) and then use whatever model you find, for subsequent labs' transmission lines. That is, we'll assume that the Thru board's transmission line's characteristic impedance might be something other than 50 ohms, but whatever we measure it to be, we'll use that per-unit-length transmission line model when designing the Lab 2 bandpass filter and the Lab 3 amplifier.

In these labs, we'll combine the above assumptions with two measurement techniques: 1) calibrating to the ends of the cables in a first-tier calibration, followed by 2) using Port Extension all the way to the 0603 component's leads (as a second-tier calibration), to derive models of parasitics. This strategy for characterizing parasitics should lead to successful circuits in the subsequent labs.

If you're interested in more advanced techniques that RF engineers use (de-embedding, etc.), there might be time at the end of the course to discuss those.

3 Lumped Passive Components

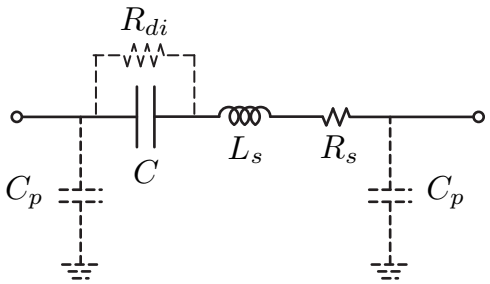

Figure 2: The lumped equivalent circuit model for a real soldered capacitor.

Up to now you have probably simulated your circuits with ideal passive components (inductors, capacitors, resistors), but real circuit components are far from ideal. Consider, for instance, a capacitor, which has an equivalent circuit model shown in Fig. 2. The model has many parasitic components which only become relevant at high frequencies. A plot of the impedance of the capacitor, shown in Fig. 3, shows that in addition to the ideal behavior, the most notable difference is the self-resonance that occurs for any real capacitor. The self-resonance is inevitable for any real capacitor due to the fact that as AC currents flow through a capacitor, a magnetic field is also generated by the capacitor, which leads to inductance

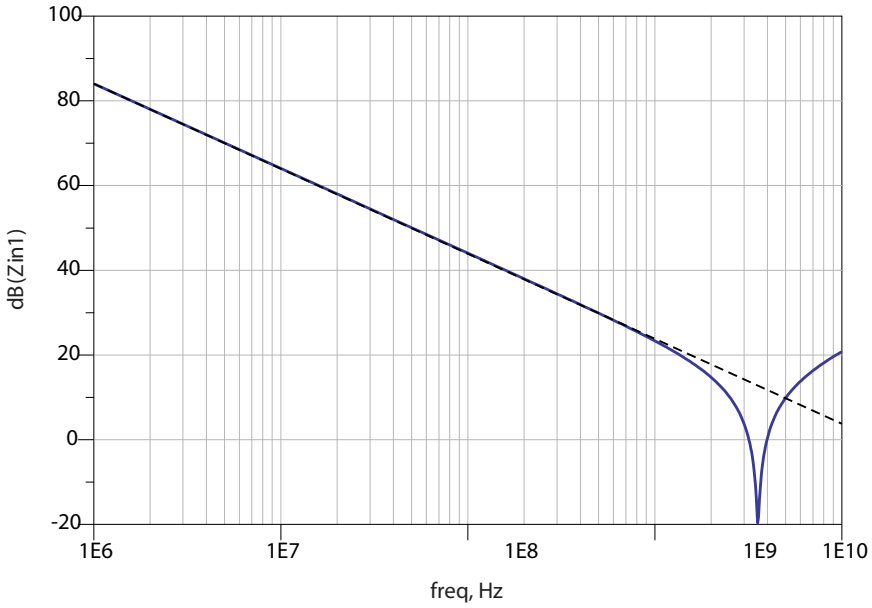

Figure 3: The magnitude of the impedance of a real capacitor (the dashed line shows the ideal behavior).

in the structure. This inductance is exacerbated by the leads of the capacitor, which often dominate the inductance. The inductive parasitics are lumped into a single inductor L_s in series with the capacitor. The finite conductivity of the plates and the leads also results in some series loss, modeled by R_s (sometimes labeled ESR, or effective series resistance). Unless a capacitor is fabricated in a vacuum, the dielectric material that separates the plates also has loss (and resonance), which is usually modeled by a large shunt resistance, R_{di}. Furthermore, when a capacitor is soldered onto a PCB, there is parasitic capacitance from the solder pads to the ground plane, resulting in the capacitors, C_p, in the equivalent model.

In a like manner, every inductor also has parasitics, as shown in the equivalent circuit model (Fig. 4), which limit operating frequency range. The series resistance, R_x, is due to the

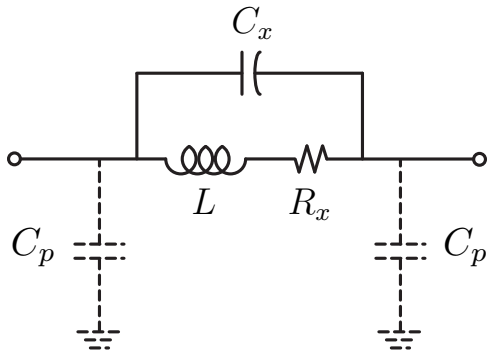

Figure 4: The lumped equivalent circuit model for a real soldered inductor.

winding resistance, and the capacitance C_x models the distributed turn-to-turn capacitance of the windings. The inductorself resonates at a frequency of approximately $1/\sqrt{LC_x}$ and has a quality factor $Q = \omega L/R_x$. When the inductor is soldered onto the PCB, there is an additional capacitance to ground modeled by C_p, which lowers the self-resonant frequency to $1/\sqrt{L(C_x + C_p/2)}$.

4 Board Parasitics

In addition to the component parasitics, you will find that there are significant parasitics associated with the PCB. When you solder a component in series between two microstrip traces on a board, the placement of the component relative to the ground plane will affect the inductance and capacitance of the component. Likewise, when you solder a component to ground, the via path will affect the inductance. There is both inductance and resistance associated with the via to the ground plane.

Traces between components act as transmission lines and can therefore be modeled as LC circuits at low frequencies if the length of the trace is much shorter than the wavelength ($\ell \ll \lambda$). For example, ideally a short circuit should have zero impedance, but as the measurements will show, there is a finite amount of inductance and resistance below the self-resonant frequency.

It is important to realize that the ground plane itself contributes resistance, especially at higher frequencies when the current flow is non-uniform and flows directly underneath the top trace of a microstrip transmission line. As explained in more detail in the next section, the "inductance" of the components is strongly related to the "return current", or the path of the current flow under the component. If the ground path beneath the component is interrupted, forcing the current to flow away from the component, the parasitic inductance increases considerably.

4.1 Component Specifications

Inductors and capacitors are often described in terms of the (1) inductance/capacitance at a particular frequency, (2) quality factor and (3) self-resonant frequency (SRF). The inductance/capacitance varies due to the non-ideal behavior of the component. For instance, the intrinsic inductance may vary with frequency due to non-uniform current flow (current crowding) at high frequencies. More prominently, though, the inductance/capacitance varies due to the complex parasitics associated with the component. Instead of specifying the equivalent circuit model, many manufacturers simply specify these two or three numbers. If the components are used well below their self-resonant frequency, these three numbers may be sufficient to characterize the structure.

The quality factor, Q, is very important in RF circuits, since it ultimately limits the performance of amplifiers, filters, and other circuits. At frequencies well below resonance, the Q factor is given by

$$Q = \frac{|X_{L|C}|}{R_x}$$

where $X_{L|C}$ is the reactance of the component at a given frequency and R_x is the effective

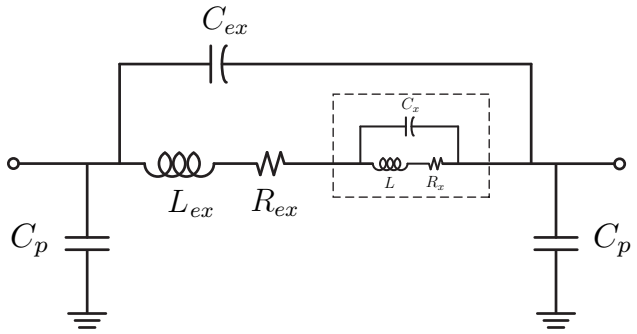

Figure 5: The lumped equivalent circuit model for an inductor includes *extrinsic* and *intrinsic* parasitic components.

series resistance (ESR) of the component. In fact, instead of Q, the ESR may be given. It's important to note that Q is a function of frequency.

The self-resonance is determined by the parasitics in the structure, and when a manufacturer of a component specifies this value, it's difficult to know what they mean! For instance, for a capacitor, the series inductance is a strong function of how the component is connected to the board. The consequent geometry will set the parasitic inductance and hence the self-resonant frequency. One can only guess how the component was characterized. For instance, if an 0603 capacitor is measured as a two-port circuit using transmission line interconnect, then inductance is a strong function of the characteristic impedance of the line's Z_0 (see below). It is therefore advisable to measure the self-resonance frequency of the component for the application at hand by measuring test structures on test boards which have similar geometry to what you'll use in your final design. RF designers often send out boards with such structures before they fab their final board designs. This way, parasitics can be characterized on the test boards, and their effects compensated for in the final design.

4.2 The Origin of Component Parasitics

As we discussed, the parasitics of a non-ideal inductor shown in Fig. 4 include series loss R_x, a "winding" capacitance C_x, and parasitic capacitance C_p. These parasitics arise from two sources: (1) intrinsic parasitics related to the way the inductor itself is physically constructed and (2) extrinsic parasitics resulting from the way the component is soldered on the PCB substrate. In the case of integrated circuit (IC) inductors, the same parasitics arise, but the extrinsic parasitics are related to the Si substrate as opposed to the PCB substrate. In Fig. 5, we divide the equivalent circuit into the intrinsic and extrinsic portion.

The intrinsic losses can be understood by examining a typical solenoidal air-core inductor used for RF applications (Fig. 6). Since the winding wire has resistance, the inductor winding must include a series resistance, R_x, in the equivalent circuit model introduced in Fig. 4. Likewise, since the windings of the inductor come in close proximity, at very high frequencies signals can skip the loop and travel directly from winding to winding through the intrinsic capacitance between the windings. This is especially true at high frequencies when the potential difference between the windings increases ($V_{diff} \propto \omega L_w$). The effect of

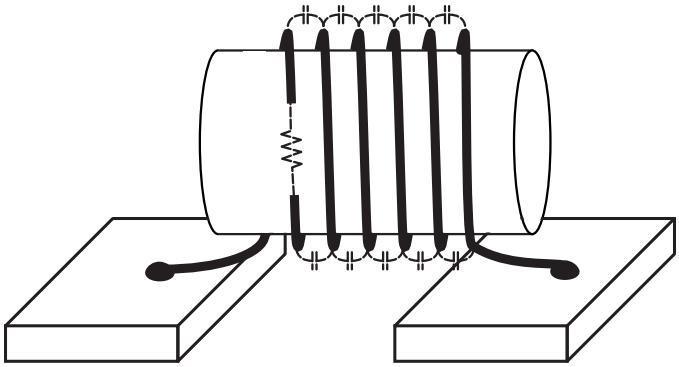

Figure 6: A solenoidal "air-core" high frequency inductor geometry.

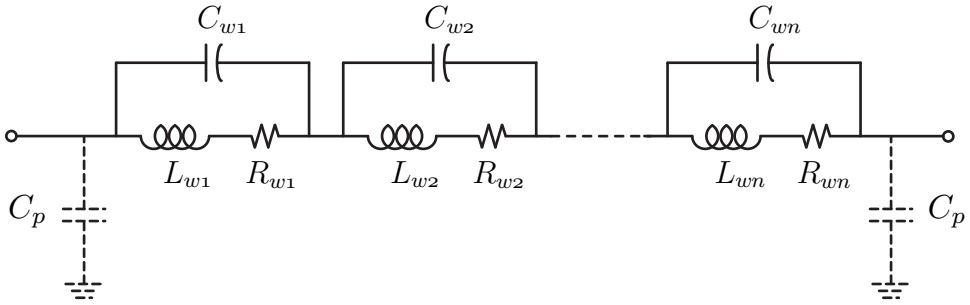

Figure 7: Distributed model for a solenoidal inductor.

the interwinding capacitance is modeled by the capacitor C_x in the equivalent circuit model.

In reality, the interwinding capacitance is distributed non-uniformly throughout the structure and a more sophisticated model, shown in Fig. 7, can be used to capture the impedance of the structure more accurately. In practice, though, this is not necessary as long as we employ the inductor well below its *self-resonant frequency* (SRF), ω_0. The SRF is defined as the frequency at which the imaginary portion of the inductor impedance $Z_L(\omega_0)$ reaches zero, $\Im\left(Z_L(\omega_0)\right) = 0$. Above this frequency the inductor begins to behave like a capacitor, as more energy is stored in the electric field rather than the magnetic field. This occurs because the signal is bypassing the windings in favor of the capacitive coupling mechanism (i.e. the interwinding capacitance).

When an inductor is used in any real circuit, it must be connected to other components through traces on the PCB, as shown in Fig. 8. Here we see that pads on the PCB are used to form the correct footprint for the inductor so that it's possible to solder the leads of the inductor to the PCB substrate. If we define the outer edges of where the inductors' leads align with the outer edges of the pads, as locations A and B, we can clearly see that capacitors C_p are needed to model the pads' capacitance to the substrate, since the back-side of the substrate is usually a ground plane.

There is a gap on the PCB between the inner edges of the pads. These locations are marked C and D in Fig. 8. A small electrical fringing field can couple across this gap as shown in Fig. 9. The presence of the ground plane greatly reduces this coupling capacitor

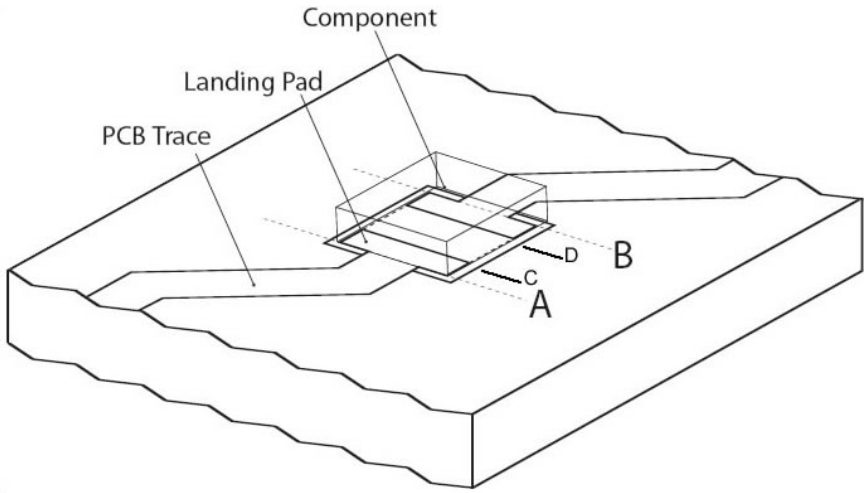

Figure 8: The footprint of an inductor on a PCB substrate consists of two landing pads. PCB traces connect each pad to other components on the board. The 0603 device which we solder onto the board has leads, which are the two metalized ends that sit on the footprint's pads. The bottom side of the board is a solid ground plane.

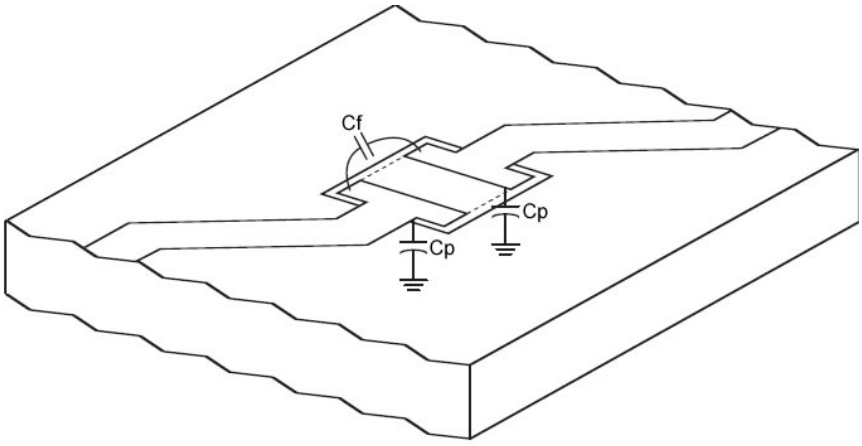

Figure 9: The capacitance between the landing pads includes a coupling capacitor due to the fringing fields between the pads.

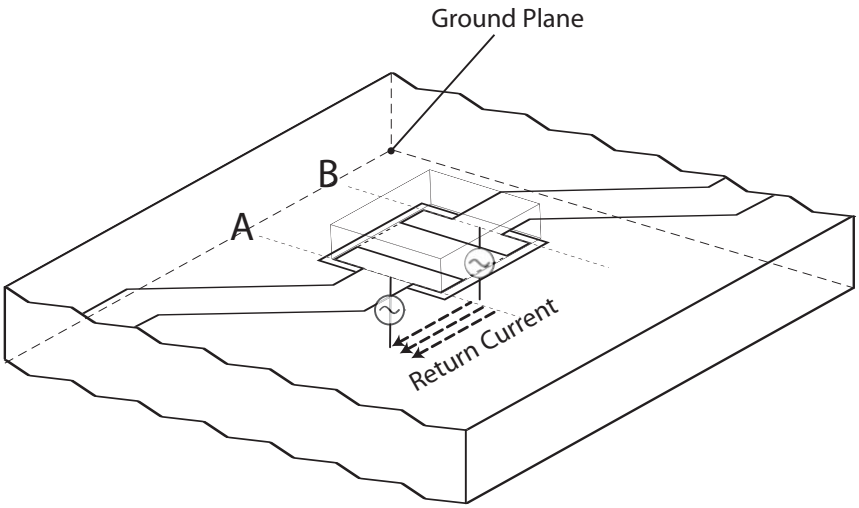

Figure 10: The return current in a PCB inductor flows through the ground plane.

C_f, but as components are reduced in physical size or if the substrate thickness is made larger, this coupling increases.

While an 0603 component's pad capacitors are easy to understand, the concept of lead inductance is much more difficult to explain. Recall that the inductance of any structure is only defined for a *closed* loop. Since the reference lines A and B are physically separated, the inductance between them must include a "return path" for the current. Imagine connecting voltage sources at locations A and B as shown in Fig. 10. Now we can see that current flows in a loop by flowing through the ground plane between A and B. This loop stores magnetic energy and thus has an inductance L_{ex}, which we incorporate into the equivalent circuit model of Fig. 5. It is important to realize that to first order, this lead inductance is independent of the inductance of the component inductor since the current flows through the same path regardless of the value of inductance L. In fact, if we short out the gap between A and B, we still experience the lead inductance L_{ex}. We therefore augment the equivalent circuit model to account for this extra *extrinsic* inductance in the component, which is a function of the layout of the component rather than the component itself. Since traces on the PCB also incur additional loss, an extra resistance, R_{ex}, has been added to the model as well.

For integrated circuits, the same considerations apply with a couple of small minor adjustments. A typical integrated inductor is made in spiral form, as shown in Fig. 11. Inter-winding resistance and coupling capacitance occur as well, but the substrate is usually quite thick compared to the dimensions of the spiral. Typically, the substrate is $700\mu m$ thick. The back of the substrate is not always an ideal ground plane (sometimes a non-conductive glue is used to attach the die to the package) and the return-current signal path is actually just below the surface of the substrate through metal layers. Since these return-current layers can be made very close to the top-metal inductor windings, the extrinsic inductance can be reduced significantly. In Fig. 12, the windings are routed in such a manner as to close the loop, effectively producing a one-port structure. The most important complication for inte-

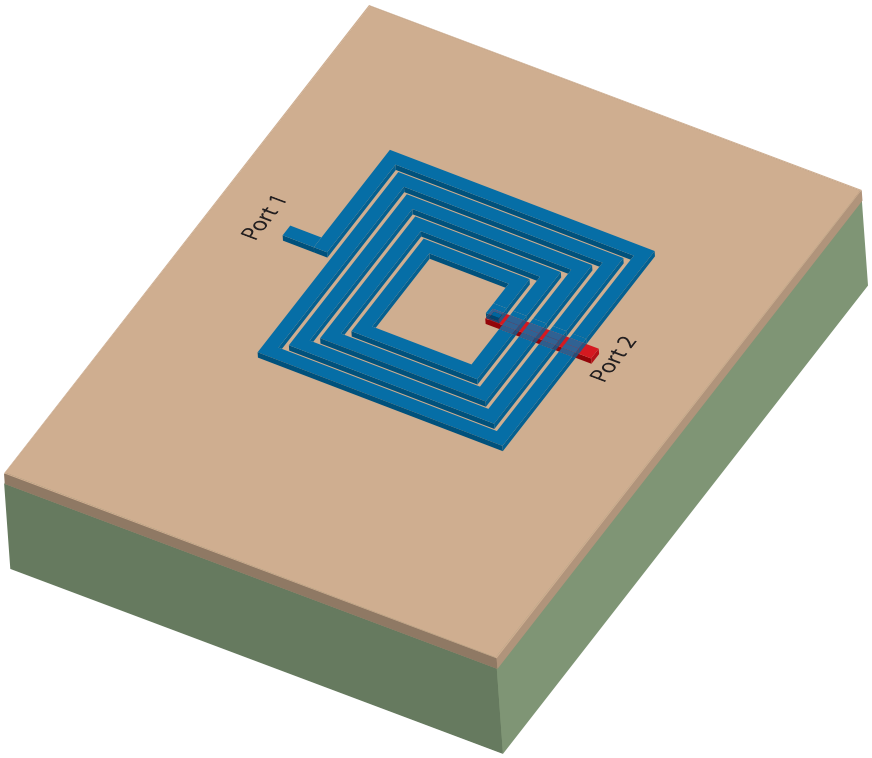

Figure 11: The layout of an on-chip spiral inductor (two-port structure, with the ground connection for each port being either the substrate of a deposited metal layer just below the top-metal layer).

grated inductors, though, arises from the capacitive coupling through a doped Si substrate (conductivity varies but a good typical value for a modern process is about 10 Ωcm), which is modeled by including series resistances, R_{sub1} and R_{sub2}, in the equivalent circuit model shown in Fig. 13. It is important to note that depending on the thickness and conductivity of the substrate, the coupling between the end leads of the inductor, through the substrate, varies significantly. An extra resistance, R_{sub3}, models the coupling through the substrate. The extra substrate capacitors, C_{sub1} and C_{sub2}, model the displacement current flow in the substrate.

It is now easy to see that all the (extrinsic and intrinsic) inductance can be lumped into a single inductor L, in Fig. 4, while all the resistance is lumped into R_x. This simpler model shown in Fig. 4 is thus adequate for capturing the high frequency behavior of the component if it is employed well below the self-resonant frequency. Near or above the SRF, the component is dominated by distributed behavior and a simple lumped circuit such as this one cannot capture the behavior.

It is now clear that other components besides inductors can be similarly divided into intrinsic and extrinsic parasitics. For instance, a large discrete capacitor is physically manufactured by sandwiching several plates and stacking or rolling the plates to realize a large capacitance in a small volume (Fig. 14). For RF applications, many capacitors are made by using a flat parallel plate structure called a metal-insulator-metal (MIM) capacitor. A very

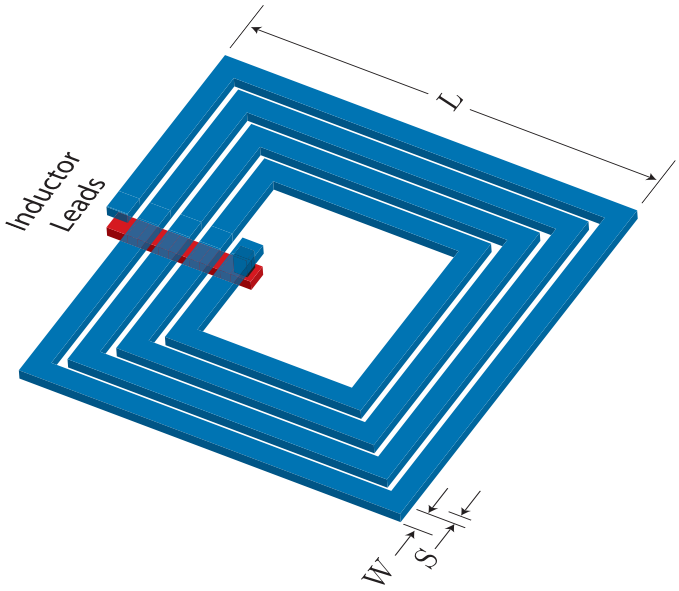

Figure 12: The layout of an on-chip spiral inductor (one-port structure, where the port is across the two ends of this winding).

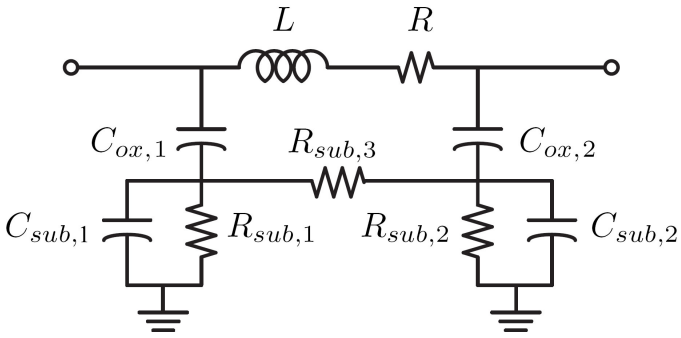

Figure 13: The model for an on-chip inductor on a lossy substrate.

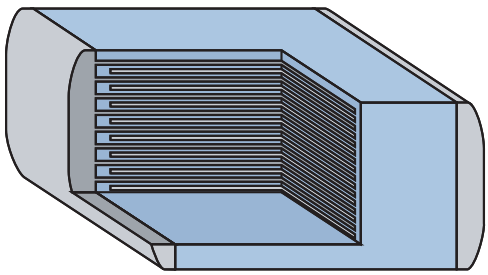

Figure 14: The physical layout of a multi-layer surface-mount capacitor. (Source: Wikipedia)

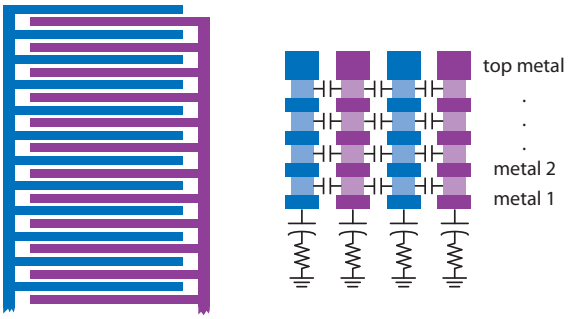

Figure 15: A MIM "finger" capacitor layout.

thin insulator is used to maximize the capacitance between the plates. In an IC process, lateral or flux capacitors use small interdigitated fingers to realize a high capacitance between the end leads of the capacitor (Fig. 15). Due the materials employed in the construction of the capacitor, we model the lead series resistance as R_s in Fig. 2. The parasitic inductance, L_s, of the capacitor is due to the magnetic energy storage in the structure when we connect a voltage source between the leads and measure the AC current flow. At high frequencies, we find that the reactive portion of the impedance increases and crosses zero at the self-resonant frequency. This behavior is modeled by the capacitor's series inductance, L_s. The value of L_s is very dependent on how we connect the capacitor's leads to other components. If the capacitor is placed on a PCB substrate, then its parasitic lead inductance is defined by the return current loop formed by the ground plane as shown in Fig. 10. As before, we account for the pad capacitances by adding capacitors, C_p, to the model.

4.3 Calculation of Component Parasitics

It is useful to estimate the parasitics of a component by using some simple assumptions. A very common layout technique in RF PCB circuits is the microstrip configuration shown in Fig. 16. Fig. 16 shows just the trace portion of the layout of Fig. 8.

Fig. 8 shows both the traces and a component footprint. There, the leads of the component would be soldered to the component's "landing pads" (which are large enough for the component to fit), which may be wider than the traces used for interconnect. If we assume that the current flows across the landing pads and through the component in the direction of the trace, and assuming there is a ground plane underneath the structure, we can model the component's parasitics as a transmission line of length ℓ, propagation constant γ, and characteristic impedance Z_{TL}. That is, even if the component is a zero ohm resistor, the mere presence of its finite-geometry footprint needs to be accounted for, and we can account for it by modeling it as a transmission line (i.e. by Z_{TL}, γ and ℓ, or equivalently by the C-L-R-C model of Fig. 17).

For any given microstrip transmission line, the characteristic impedance, Z_{TL}, can be calculated using standard tables or approximate equations (online tools are also available) once the the width and height of the microstrip line are specified. From transmission line theory, the equivalent circuit for a short section of transmission line $\ell \ll \lambda$ is given by Fig. 17,

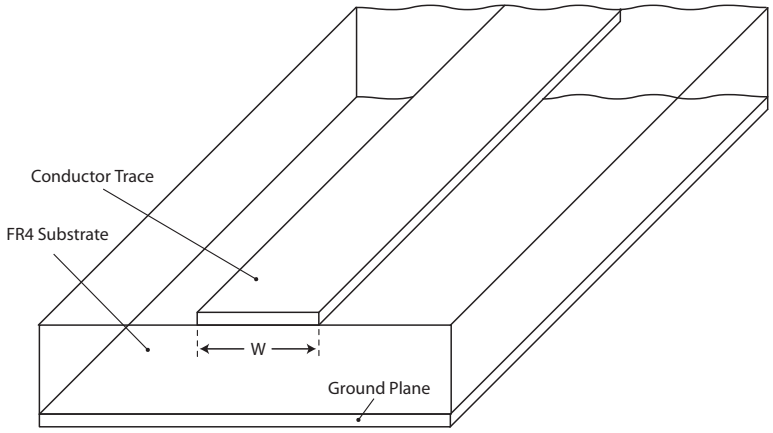

Figure 16: A microstrip transmission line formed on a PCB substrate.

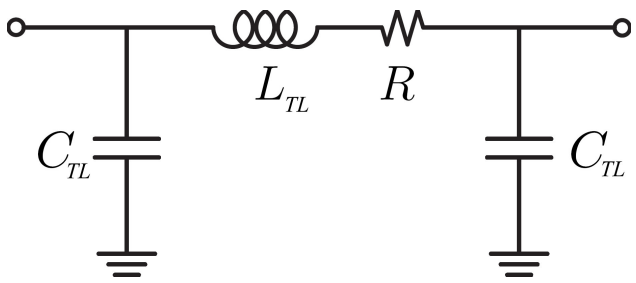

Figure 17: An equivalent circuit for a short section of a lossy transmission line, such as a microstrip line on FR4.

where λ is the quasi-TE mode propagation wavelength in the PCB. If the dielectric constant of the PCB is much larger than the dielectric constant of air, then the wave propagates mostly in the PCB medium, with a velocity $v = c/\sqrt{\epsilon_{re}}$, where ϵ_{re} is the effective relative dielectric constant for microstrip geometry. More accurate values of v can be obtained from approximate equations or tables.

The modeling component values for a transmission line for the Fig. 17 model (ignoring loss) are calculated as follows

$$\omega L_{TL} \approx Z_{TL}\beta\ell = Z_{TL}2\pi\frac{\ell}{\lambda}$$

$$\omega C_{TL} \approx \frac{1}{2}Y_{TL}\beta\ell = Y_{TL}\pi\frac{\ell}{\lambda}$$

Here, for a lossless model, we've assumed that the attenuation constant, α, in the expression for the complex propagation constant, $\gamma = \alpha + j\beta$, is zero.

At 1 GHz, the wavelength in free-space is 30 cm, and in the PCB it's 15 cm. That is, since the relative dielectric constant of FR4 is about 4, the velocity of the wave in the FR4 transmission line will be $1/sqrt(4)$ of the velocity of light in vacuum, or half of 3×10^8 m/s. An 0603 component is 60 mils long (and 30 mils wide), or about 1.5 mm long, which is only 1% of the wavelength. Therefore, our lumped circuit model for the transmission line will be reasonably accurate. Assuming $Z_{TL} = 50\Omega$, then the inductance is approximately given by $L_{TL} = 0.5$ nH. Typically, the landing pads of a footprint are designed to extend a bit beyond the length of the 0603 part so that a solder fillet has room to make a toe on each end of the component. As an estimate, let's assume the pads make the overall footprint be 120 mils by 30 mils (i.e. twice as long as the 0603 part itself). In this case, the modeling inductance is double what we just calculated, or about 1 nH. The modeling capacitance is $C_{TL} = 1$ fF. With this method then, we can model the parasitics due to the space that the 0603 component takes up on the board (i.e. the 120 mil by 30 mil footprint). This calculation has assumed that that component and its pads were wider than the trace width (as shown in the earlier figures), which holds for 0603 parts when the substrate is very thin. Our boards are rather thick and the 0603 components are actually skinnier than the trace width so you would modify the modeling steps accordingly.

If the length of the transmission line approaches a significant fraction of the wavelength, then a more accurate model of a component's parasitics can be employed. The Y parameters of the transmission line are given by

$$Y_{11} = Y_{22} = Y_o \coth(\gamma\ell)$$

$$Y_{12} = Y_{21} = -Y_0 \mathrm{csch}(\gamma\ell)$$

where $\gamma = \alpha + j\beta$ is the complex propagation constant (including loss). The complex hyperbolic functions can be calculated by

$$\coth(\gamma\ell) = \frac{\cosh(\alpha\ell)\cos(\beta\ell) + j\sinh(\alpha\ell)\sin(\beta\ell)}{\sinh(\alpha\ell)\cos(\beta\ell) + j\cosh(\alpha\ell)\sin(\beta\ell)}$$

$$\mathrm{csch}(\gamma\ell) = \frac{1}{\sinh(\gamma\ell)} = \frac{1}{\sinh(\alpha\ell)\cos(\beta\ell) + j\cosh(\alpha\ell)\sin(\beta\ell)}$$