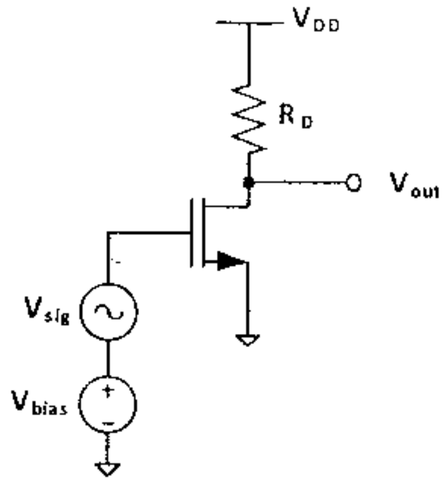
1. In the following circuit, assuming that the transistor is operating in the saturation region:

a) Find the required V_{bias} for which the dc value of the V_{out} is 1.5 V. **[10 marks]**

b) Is the assumption that the transistor is in the saturation region correct? **[4 marks]**

c) Find the small-signal gain V_{out}/V_{sig}. **[6 marks]**

Assume $\lambda = 0$, $\gamma = 1V^{1/2}$, $2\Phi_F$=0.64V, V_{TH0}= 0.5V, $\mu_n C_{ox} = 1\ mA/V^2$, $(W/L)_{NMOS} = 48$, $R_D = 1\ k\Omega$, and V_{DD}= 3.0 V.



No body effect

a) $I_D = \frac{V_{dd} - V_{out}}{R_D} = \frac{3 - 1.5}{1K} = 1.5\ mA$

$I_D = 1.5\ mA = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{bias} - V_{th})^2 \rightarrow 1.5 = \frac{1}{2} \times 1 \times 48\,(V_{bias} - 0.5)^2$

$\rightarrow \boxed{V_{bias} = 0.75\ V}$

b) $V_{GD} = V_{bias} - V_{out} = 0.75 - 1.5 < V_{th} \rightarrow$ The device is in sat.

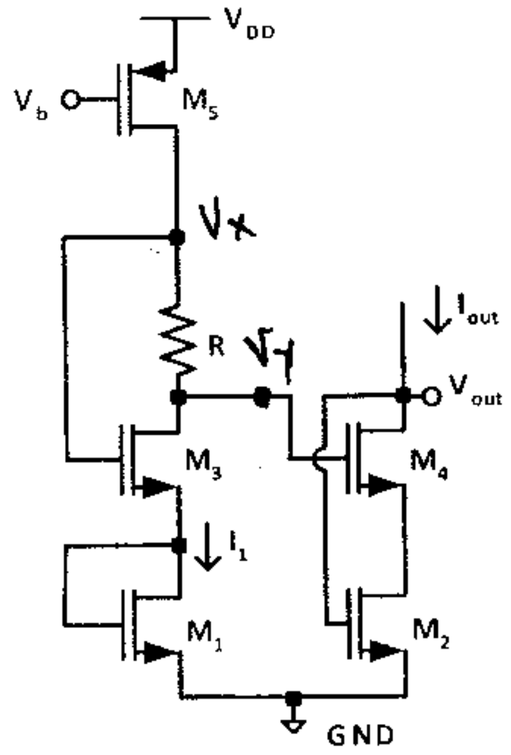
c) $A_V = -g_m \cdot R_D$

$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th}) = 1 \times 48 \times 0.25 = 12\ \frac{mA}{V}$

$\Rightarrow \boxed{A_V = -12 \times 1 = -12\ \frac{V}{V}}$

2. In the follwing circuit assume that:
$\lambda_{(NMOS)} = \lambda_{(PMOS)} = 0V^{-1}$, $\gamma = 0$, $V_{DD} = 3$ V, $V_b = 2.3$ V, $V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.5$V, $\mu_n C_{ox} = 1$ mA/V^2, $\mu_p C_{ox} = 0.25$ mA/V^2.

Furthermore, assume that $I_1 = I_{out}$ and all transistors have the same size ($\frac{W}{L} = 40$). Find the value of R that results in the minimal voltage headroom required at node V_{out}. **[20 marks]**



$$I_{out} = I_5 = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)(V_{SG_5} - |V_{th}|)^2 = \frac{1}{2} \times 0.25 \times 40 (3 - 2.3 - 0.5)^2 = 0.2 \text{ mA}$$

$$I_1 = I_{out} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS_1} - V_{th})^2 \longrightarrow 0.2\,\text{mA} = \frac{1}{2} \times 1 \times 40 (V_{GS_1} - 0.5)^2$$

$$\longrightarrow V_{GS_1} = V_{GS_3} = V_{GS_2} = V_{GS_4} = 0.6\,V \quad , \quad V_{out} = V_{GS_2} = 0.6\,V$$

M_2 must be biased at the edge of saturation, therefore $V_{GD_2} = V_{th} \longrightarrow$

$$V_{out} - V_{D_2} = 0.5 \longrightarrow 0.6 - V_{D_2} = 0.5 \longrightarrow \boxed{V_{D_2} = 0.1\,V}$$

$$\begin{cases} V_Y = V_{G_4} = V_{D_2} + V_{GS_4} = 0.1 + 0.6 = 0.7\,V \\ V_X = V_{G_3} = V_{D_1} + V_{GS_3} = V_{GS_1} + V_{GS_3} = 0.6 + 0.6 = 1.2\,V \end{cases}$$

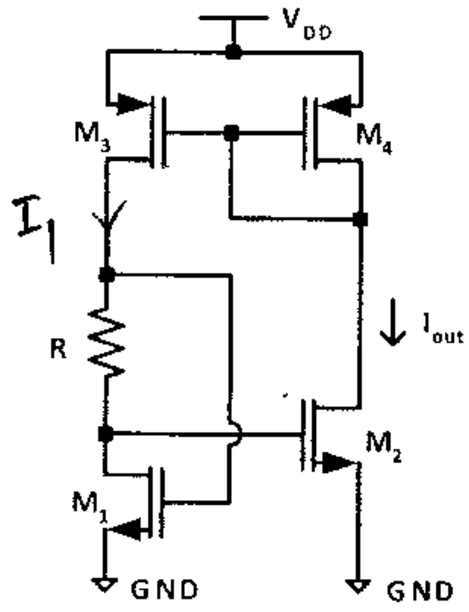
$$R = \frac{V_X - V_Y}{I} = \frac{1.2 - 0.7}{0.2\,mA} = \boxed{2.5\,K\Omega}$$

3. Assumibng that all transistors are in saturation, $\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4$, and $\lambda = \gamma = 0$:

i) Find an expression for I_{out} in terms of R, transistor parameters (e.g., μ and C_{ox}), and transistor sizes **[10 marks].**

ii) What would be the percentage change in I_{out} if V_{DD} is increased by 10%. **[5 marks]**

iii) How would the expression for I_{out} derived in part (i) change if $\gamma \neq 0$ and why? **[5 marks]**



i) $I_1 = I_{out}$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS_2} - V_{th_n})^2 \longrightarrow V_{GS_2} = V_{th_n} + \sqrt{\frac{2I_{out}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_2}}$$

$$\text{Similarly: } V_{GS_1} = V_{thn} + \sqrt{\frac{2\,I_{out}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}}$$

$$V_{GS_1} - V_{GS_2} = R\,I_{out} \longrightarrow \sqrt{\frac{2\,I_{out}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} - \sqrt{\frac{2\,I_{out}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_2}} = R\,I_{out} \longrightarrow$$

$$R\sqrt{I_{out}} = \sqrt{\frac{2}{\mu_n C_{ox}}}\left(\sqrt{\left(\frac{L}{W}\right)_1} - \sqrt{\left(\frac{L}{W}\right)_2}\right) \longrightarrow I_{out} = \frac{2}{\mu_n C_{ox} R^2}\left[\sqrt{\frac{L_1}{W_1}} - \sqrt{\frac{L_2}{W_2}}\right]^2$$

ii) no change, I_{out} does not depend on VDD.

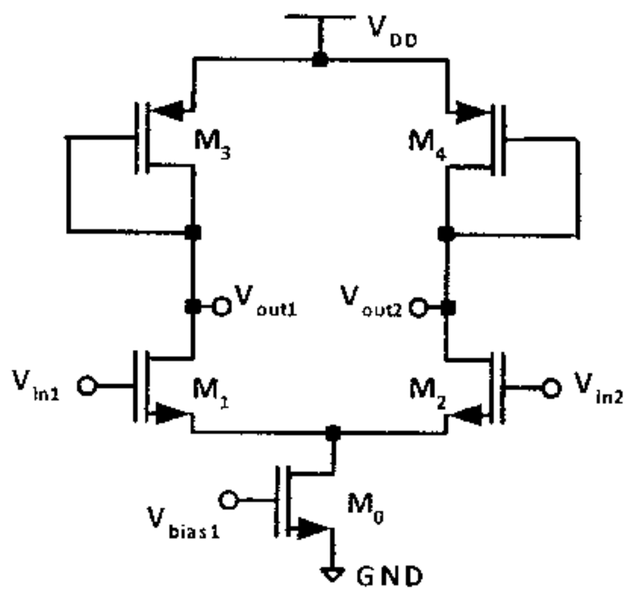
iii) no change, there is no body effect ($V_{SB_1} = V_{SB_2} = 0$)

4. Design a symmetric differential amplifier based on the topology shown below with the following design specifications:

- V_{DD}=3.0 V
- Total power consumption of 3.0 mW
- Output DC level of 1.5 V
- Differential gain of 40 V/V
- L =0.4 μm for all devices

Assume that the minimum required voltage at the drain of M_0 to keep it in saturation is 0.2 V.

The technology parameters are:
$\lambda_{(NMOS)}=0\ V^{-1}$, $\lambda_{(PMOS)}=0V^{-1}$, $\gamma=0$, $V_{DD}=3.0$ V, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.5V$, $\mu_nC_{ox}=1mA/V^2$, $\mu_pC_{ox}=0.25\ mA/V^2$.



a) Find V_{bias1}, and all the transistor widths (i.e., W_0,W_1, W_2, W_3, and W_4). **[14 marks]**
b) Find the minimum and maximum allowable input common-mode (input DC) levels **[6 marks]**.

a) M_0 is biased at the edge of the sat. region, therefore $V_{GD_0} = V_{th}$

$\longrightarrow V_{bias_1} - 0.2 = 0.5V \longrightarrow \boxed{V_{bias_1} = 0.7V}$

$$I_{M_0} = \frac{P}{V_{DD}} = \frac{3mW}{3V} = 1mA$$

$$I_3 = \frac{I_{M_0}}{2} = 0.5\ mA = \frac{1}{2} \times 0.25 \times \frac{W_3}{0.4} (3 - 1.5 - 0.5)^2 \longrightarrow \boxed{W_3 = W_4 = 1.6\ \mu m}$$

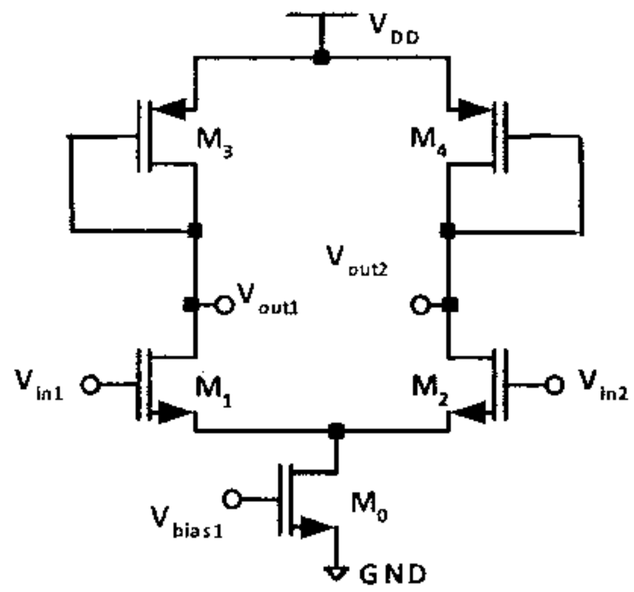
$$I_{M_0} = \frac{1}{2}\mu_n C_{ox} \frac{W_0}{L} (V_{bias_1} - V_{th})^2 \longrightarrow 1mA = \frac{1}{2} \times 1 \times \frac{W_0}{0.4} \times (0.7 - 0.5)^2 \longrightarrow \boxed{W_0 = 20\ \mu m}$$

$$g_{m3} = \mu_p C_{ox} \left(\frac{W}{L}\right)_3 (V_{SG3} - |V_{th}|) = 0.25 \times \frac{1.6}{0.4} \times 1 = 1\ \frac{mA}{V}$$

$$A_V = -\frac{g_{m1}}{g_{m3}} = -40 \longrightarrow \frac{g_{m1}}{1} = 40 \longrightarrow g_{m_1} = 40\ \frac{mA}{V}$$

$$g_{m_1} = 40 = \sqrt{2 K_n I_{D_1}} = \sqrt{2 \times 1 \times \frac{W_1}{0.4} \times 0.5} \longrightarrow \boxed{W_1 = 640\ \mu m} = W_2$$

For your convenience the circuit diagram and transistor parameters are replicated here:
$\lambda_{(NMOS)}=0\ V^{-1}$, $\lambda_{(PMOS)}=0V^{-1}$, $\gamma=0$, $V_{DD}=3.0\ V$, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.5V$, $\mu_n C_{ox}=1mA/V^2$, $\mu_p C_{ox}=0.25\ mA/V^2$.



$$I_{D_1} = 0.5\,mA = \frac{1}{2} \times 1 \times \frac{640}{0.4} (V_{GS_1} - 0.5)^2 \longrightarrow V_{GS_1} = 0.525\ V$$

$$V_{in\,CM\,min} = V_{D_0\,min} + V_{GS_1} = 0.2 + 0.525 = 0.725\ V$$

$V_{in\,CM\,max}$: M_1 must stay in saturation for the maximum input voltage.

$$V_{GD_1} \leq V_{th} \longrightarrow V_{in\,CM\,max} - V_{out} \leq V_{th} \longrightarrow$$

$$V_{in\,CM} - 1.5 \leq 0.5 \longrightarrow V_{in\,CM\,max} = 2\ V$$