Quiz 1
Tuesday February 5, 2008
EECE 488: Analog CMOS Integrated Circuit Design
Time: 80 minutes

Name:

Student Number: Solutions.

Note: The Quiz has two questions. Please answer all questions in the space provided.

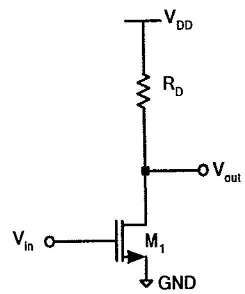
Good luck!

1. Design a common-source amplifier with a resistive load based on the schematic shown below with the following design specifications:

- V_{DD}=1.8V
- Transistor M_1 is in saturation
- The minimum possible output voltage to keep M_1 in saturation is 0.2V
- Total power consumption of the amplifier is 0.9mW
- Absolute value of gain of 10
- L=0.4μm for the transistor

The technology parameters are:

$\lambda_{(NMOS)} = 0$, $\gamma = 0$, V_{DD}=1.8V, $V_{TH(NMOS)} = 0.4V$, $\mu_n C_{ox}$=1 mA/V^2 .



Find the following values:

1) DC level of the input **(2 marks)**
2) Width (W_1) of transistor M_1 **(2 marks)**
3) R_D **(2 marks)**
4) Nominal dc level (bias level) of the output node **(2marks)**
5) Maximum output signal swing for a symmetric output signal **(2marks)**

1.) The transistor is in saturation as long as $V_{DS} \geq V_{GS} - V_{TH}$. We are told that the transistor leaves saturation when V_{DS} falls below 0.2V.

$\Rightarrow 0.2 = V_{GS} - V_{TH} \Rightarrow \underline{V_{GS}} = 0.2 + 0.4 = \underline{\underline{0.6V}}$

and $\underline{V_{eff} = 0.2V}$.

2.) From part (1) we know V_{eff}, and we can find I_D from the specified power consumption:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{eff}^2 = \frac{P}{V_{DD}} = \frac{0.9\,mW}{1.8\,V} = 0.5\,mA$$

$$W = \frac{2L\,I_D}{\mu_n C_{ox} V_{eff}^2} = \underline{\underline{10\,\mu m}}$$

3.) From the gain and g_m we can find R_D:

$$|A_v| = g_m R_D = 10 \quad , \quad g_m = \mu_n C_{ox}\frac{W}{L}V_{eff} = \frac{2I_D}{V_{eff}}$$

$$= 5\times10^{-3}\ A/V.$$

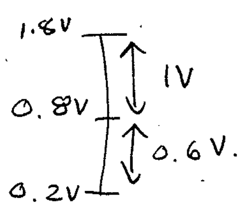
$$R_D = \frac{10}{g_m} = \underline{\underline{2\,K\Omega.}}$$

4.) From the bias current and R_D we can find the DC level of V_{out}:

$$V_{out} = V_{DD} - I_D R_D = 1.8 - (0.5\times10^{-3})(2\times10^{3})$$

$$= 1.8 - 1 = \underline{\underline{0.8\,V}}$$

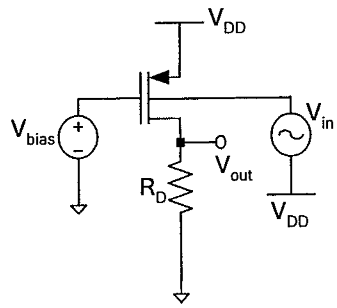
5.) The output signal can not swing above V_{DD} or below the specified 0.2V.



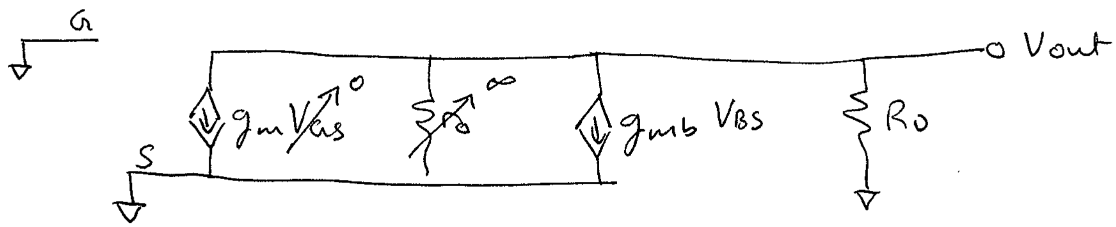
$\Rightarrow$ Maximum symmetric output swing is $\underline{\underline{\pm\,0.6\,V}}$

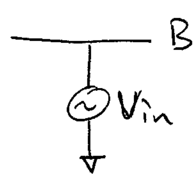
2. It is possible to use the <u>bulk terminal</u> of a transistor as an input of an amplifier. Consider the single-stage PMOS amplifier shown below. For V_{bias}=1.4V, calculate the small-signal gain ($A_v=V_{out}/V_{in}$) of the amplifier. Recall that $g_{mb}=\eta g_m$.
Assume, λ = 0, η=0.2, $V_{TH(PMOS)}$= -0.6V, $\mu_p C_{ox}$=100 $\mu A/V^2$, R_D=1kΩ, $(W/L)_{PMOS}$= 20, and V_{DD}=3V. **[10 marks]**

Note: In this problem, the technology parameters are different from those of Question 1.



The small-signal model can be drawn as:





$$\Rightarrow A_V = -g_{mb} R_D.$$

For PMOS: $V_{eff} = V_{SG} - |V_{TH}| = 3 - 1.4 - 0.6 = 1\,V$

$$g_{mb} = \eta g_m = \eta \mu_p C_{ox} \frac{W}{L} V_{eff}.$$

$$= (0.2)(100\times10^{-6})(20)(1) = 0.4\times10^{-3}\,A/V.$$

$$\Rightarrow A_V = -g_{mb} R_D = -(0.4\times10^{-3})(1\times10^{3}) = \underline{\underline{-0.4\ V/V}}$$

(Can quickly check bias current:

$$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}V_{eff}^2 = \left(\frac{1}{2}\right)(100\times10^{-6})(20)(1) = 1mA.$$

$\Rightarrow V_{out} = 1V \Rightarrow V_{SD} = 2\,V \Rightarrow$ In saturation.)

Write your answer in this box

$A_v = \underline{-0.4}$ V/V

Alternatively, knowing $I_D = 1mA$:

$$g_{mb} = \eta \frac{2I_D}{V_{eff}} = 0.4 \times 10^{-3} \text{ A/V} \text{ as before.}$$