1. In the following circuit assume transistors \( M_1 \) and \( M_2 \), and transistors \( M_3 \) and \( M_4 \) are identical and \( \gamma = 0 \) and \( \lambda \neq 0 \):
   i) Find the expression for the small-signal differential voltage gain \( \frac{V_{out}}{V_{in1} - V_{in2}} \) of the circuit.
   ii) What is the gain of the circuit at very low frequencies?
   iii) What is the gain of the circuit at very high frequencies?

2. Assuming that all transistors are in saturation, \( \frac{W}{L} = \frac{W}{L} \), and \( \lambda = \gamma = 0 \):
   i) Find an expression for \( I_{out} \).
   ii) What would be the percentage change in \( I_{out} \) if \( V_{DD} \) is increased by 10%.
   iii) How would the expression for \( I_{out} \) derived in part (i) change if \( \gamma \neq 0 \) and why?
3. Design a two-stage differential-to-single-ended amplifier based on the topology shown below with the following design specifications:
- \( V_{DD} = 3 \) V
- Total power consumption of 3 mW
- Output swing of 2.6 V
- Total gain of 1000
- \( L = 0.4 \mu m \) for all the device

Use the following assumptions for your design
- Allocate equal overdrive voltages to \( M_5 \) and \( M_6 \)
- Assume the bias currents of the first stage and the second stage are equal.
- \( V_{SG3} = V_{SG5} \)

The technology parameters are:
\[
\lambda_{(NMOS)} = \lambda_{(PMOS)} = 0.1 \text{ V}^{-1}, \quad \gamma = 0, \quad V_{DD} = 3 \text{ V}, \quad V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.5 \text{ V}, \quad \mu_n C_{ox} = 1 \text{ mA/V}^2, \quad \mu_p C_{ox} = 0.5 \text{ mA/V}^2.
\]

**Note**: Use the parameter \( \lambda \) only for calculating the \( r_o \) of the transistors. **Do not** use \( \lambda \) in any other calculation including your bias currents.

Find \( V_{bias1} \), and all the transistor widths (i.e., \( W_0, W_1, W_2, W_3, W_4, W_5, W_6 \)).