EECE488 Analog CMOS Integrated Circuit Design
Assignment 4
Due: Thursday March 28, 2013 at 9:30am

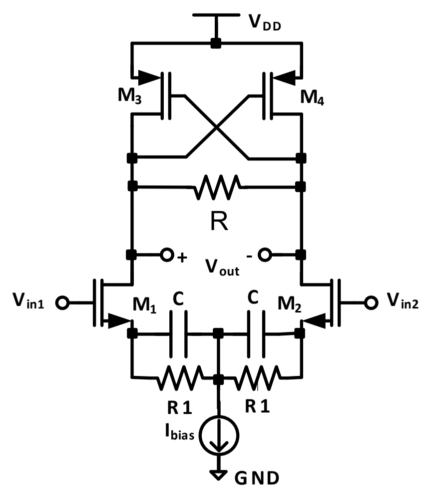
1. Assuming that the following circuit is symmetrical and $\gamma = \lambda = 0$:

i) Find the expression for the small-signal differential voltage gain ($\frac{V_{out}}{V_{in1} - V_{in2}}$) of the circuit at very low frequencies.

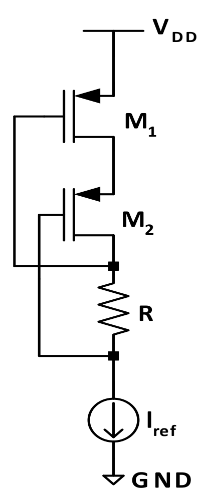
ii) What is the gain of the circuit at very high frequencies?

iii) Repeat parts (i) and (ii) assuming $\lambda \neq 0$.

Note: In this question neglect all other capacitances that are not shown in the circuit.



2. In the following cascode circuit (typically referred to as self-biased cascode circuit) the resistor R is used to maintain a proper voltage to allow both M_1 and M_2 remain in saturation.



Assume both M_1 and M_2 have the same size W/L. Ignoring the channel length modulation and the body effect, show that for M_1 and M_2 to remain in the saturation region we should have:

$$\frac{2}{\mu_p C_{ox}\left(\frac{W}{L}\right)R^2} \leq I_{ref} \leq \frac{|V_{tp}|}{R}$$

3. Design a two-stage amplifier based on the topology shown below with the following design specifications:

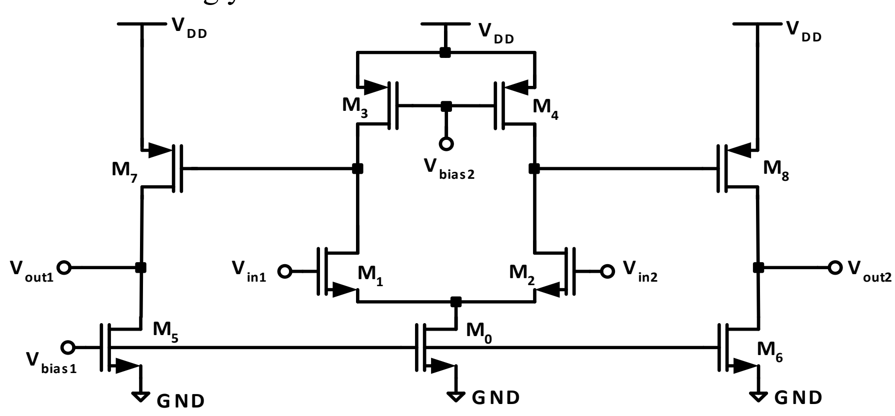
- V_{DD}=1.8V
- Total power consumption of 1.8 mW
- Differential output swing of 2.8V
- Total gain of 1000
- L=0.4μm for all the device

Use the following assumptions for your design

- The circuit is symmetric
- The bias currents of the first stage and second stage are equal (i.e., $I_0=I_5+I_6$).
- The magnitude of overdrive voltages of M_4, M_6, and M_8 are equal

The technology parameters are:
$\lambda_{(NMOS)}=\lambda_{(PMOS)}=0.1V^{-1}$, $\gamma = 0$, V_{DD}=1.8V, $V_{TH(NMOS)}=|V_{TH(PMOS)}|$=0.4V, $\mu_n C_{ox}$=0.5 mA/V^2, $\mu_p C_{ox}$=0.25 mA/V^2.

Note: Use the parameter λ only for calculating the r_o of the transistors. **Do not** use λ in any other calculation including your bias currents.



Find V_{bias1}, V_{bias2}, and all the transistor widths (i.e., W_0,W_1, W_2, W_3, W_4, W_5, W_6, W_7, and W_8).

4. The unity-gain closed-loop buffer has a phase margin of 50°. What is the percentage of peaking in magnitude frequency response of the closed-loop system in the vicinity of the gain crossover frequency (i.e., the frequency at which the loop-gain is 1)?

Good luck