5.19. The circuit shown in Fig. 5.43 exhibits a negative input capacitance. Calculate the input impedance of the circuit and identify the capacitive component.

![Figure 5.42](image)

6.6. Neglecting other capacitances, calculate the input impedance of each circuit shown in Fig. 6.36.

![Figure 6.36](image)

6.7. Estimate the poles of each circuit in Fig. 6.37.

![Figure 6.37](image)
6.9. Calculate the gain of each circuit in Fig. 6.39 at very low and very high frequencies. Neglect all other capacitances and assume $\lambda = 0$ for circuits (a) and (b) and $\gamma = 0$ for all of the circuits.

(a) \hspace{2cm} (b) 
\hspace{2cm} (c) \hspace{2cm} (d) 

Figure 6.39

6.10. Calculate the gain of each circuit in Fig. 6.40 at very low and very high frequencies. Neglect all other capacitances and assume $\lambda = \gamma = 0$.

(a) \hspace{2cm} (b) 

Figure 6.40
6.11. Consider the cascode stage shown in Fig. 6.41. In our analysis of the frequency response of a cascode stage, we assumed that the gate-drain overlap capacitance of $M_1$ is multiplied by $g_m(1/g_m + g_{mb})$. Recall from Chapter 3, however, that with a high resistance loading the drain of $M_2$, the resistance seen looking into the source of $M_2$ can be quite high, suggesting a much higher Miller multiplication factor for $C_{GD1}$. Explain why $C_{GD1}$ is still multiplied by $1 + g_m(1/g_m + g_{mb})$ if $C_L$ is relatively large.

![Figure 6.41](image)

6.12. Neglecting other capacitances, calculate $Z_\lambda$ in the circuits of Fig. 6.42. Sketch $|Z_\lambda|$ versus frequency.

![Figure 6.42](image)

6.14. Suppose in the cascode stage of Fig. 6.25, a resistor $R_G$ appears in series with the gate of $M_2$. Including only $C_{GS2}$, neglecting other capacitances, and assuming $\lambda = \gamma = 0$, determine the transfer function.

![Figure 6.25](image)
9.7. Design the op amp of Fig. 9.21 for the following requirements: maximum differential swing = 4 V, total power dissipation = 6 mW, \( I_{SS} = 0.5 \) mA. 

![Figure 9.21 Simple implementation of a two-stage op amp.](image)

9.18. In this problem, we design a two-stage op amp based on the topology shown in Fig. 9.68. Assume a power budget of 6 mW, a required output swing of 2.5 V, and \( L_{eff} = 0.5 \mu m \) for all devices.

![Figure 9.68](image)

9.22. It is possible to use the bulk terminal of PMOS devices as an input [9]. Consider the amplifier shown in Fig. 9.69 as an example.

![Figure 9.69](image)

(a) Calculate the voltage gain.
(b) What is the acceptable input common-mode range?
(c) How does the small-signal gain vary with the input common-mode level?
(d) Calculate the input-referred thermal noise voltage and compare the result with that of a regular PMOS differential pair having NMOS current-source loads.
9.23. The idea of the active current mirror can be applied to the output stage of a two-stage op amp as well. That is, the load current source can become a function of the signal. Figure 9.70 shows an example [10]. Here, the first stage consists of $M_1$-$M_4$ and the output is produced by $M_5$-$M_8$. Transistors $M_7$ and $M_8$ operate as active current sources because their current varies with the signal voltage at nodes $Y$ and $X$, respectively.
(a) Calculate the differential voltage gain of the op amp.
(b) Estimate the magnitude of the three major poles of the circuit.

![Figure 9.70](image)

9.24. The circuit of Fig. 9.71 employs a fast path ($M'_1$ and $M'_2$) in parallel with the slow path. Calculate the differential voltage gain of the circuit. Which transistors typically limit the output swing?

![Figure 9.71](image)