EECE 488: Analog CMOS Integrated Circuit Design
Assignment 1
Due: Tuesday, February 14, 2012 at 9:30am

1. The transit frequency, f_T, of a MOS transistor is defined as the frequency at which the small-signal current gain of the device drops to unity while the source and drain terminals of the device are held at ac ground.

a) Given that in the subthreshold region the drain current of the device is:

$$I_D = I_0 e^{\frac{V_{GS}}{\eta V_T}}$$

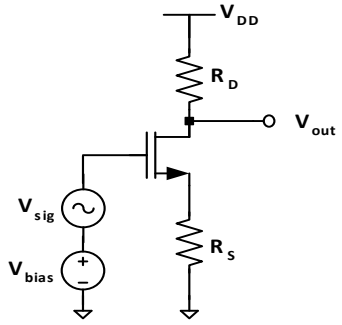
where $\eta \approx 1.5$ and $V_T = kT/q$ ($V_T = 26mV$ at the room temperature), find an expression for the f_T of a MOS device that is operating in the subthreshold region.

b) Compare the result of part (a) with the f_T of the same transistor operating in the active region and comment on the relative value of f_T of the transistor when it is operating in active region compared to when it is in subthreshold region.

2. In the following circuit, assuming that the transistor is operating in the saturation region:

a) Find the required Vbias for which the dc value of the Vout is 1.44V.
b) Is the assumption that the transistor is in the saturation region correct?
c) Find the small-signal gain V_{out}/V_{sig}.

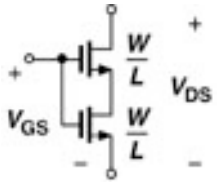
Assume $\lambda = 0$, $\gamma = 1V^{1/2}$, $2\Phi_F = 0.64V$, $V_{TH0} = 0.4V$, $\mu_n C_{ox} = 800\ \mu A/V^2$, $(W/L)_{NMOS} = 20$, $R_D = R_S = 0.5k\Omega$, and $V_{DD} = 1.8V$.



3. Use HSPICE and our 0.35-μm CMOS technology to:

a) Verify whether two identical NMOS transistors (or two PMOS transistors) each having an aspect ratio of W/L when connected in parallel behave similar to a single NMOS (PMOS) transistor with the aspect ratio of 2W/L.

b) Verify whether the structure shown below (sometimes referred to as series combination of two transistors) can be viewed as a single transistor of size W/(2L).



Good luck!