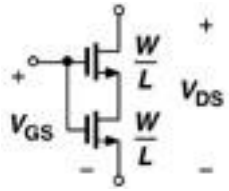
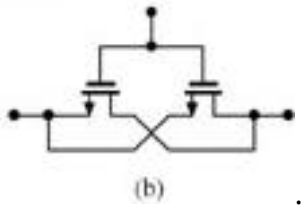
EECE488 Analog CMOS Integrated Circuit Design
Assignment 1
Due: Tuesday February 12th, 2013 at 9:30am

1. Based on Problem 2.16 of the Razavi's book:
a) Consider the structure shown in the following figure. Determine I_D as a function of V_{GS} and V_{DS} and prove that the structure can be viewed as a single transistor having an aspect ratio $W/(2L)$. Assume $\lambda = \gamma = 0$.

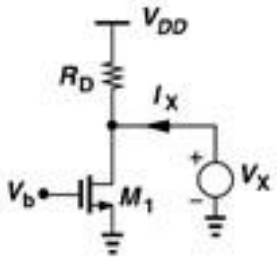


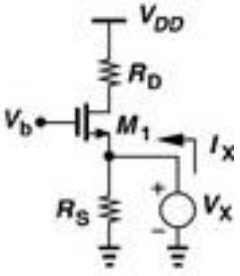
b) Repeat part a for the following structure (assuming both transistors have the same aspect ratio W/L) and show that the structure can be viewed as a single transistor having an aspect ratio of $2W/L$.

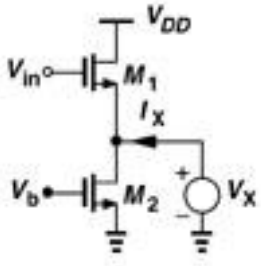

(b)

2. a) Use HSPICE and the 0.35µm CMOS technology library used in our class to plot I_D versus V_{DS} of an NMOS transistor with W=3.5 µm and L=0.35 µm when its V_{GS} is 1 V or 2 V. For each V_{GS} use two difference V_{BS} of 0V and -1V.
b) Assuming that long channel quadratic equations for I_D holds, use the information from the I_D plots in part (a) to calculate a rough estimate of the process parameters V_{th0}, $\mu_n C_{ox}$, γ and λ for the transistor you used in part (a).
c) For V_{BS}=0, calculate g_m of the transistor in part (a) for each value of V_{GS} based on your estimated process parameters in part b and long channel equations discussed in class. Compare the estimated g_m values with those calculated by HSPICE (using gmo) and calculate the relative error.

3. Calculate the output resistance (V_X/I_X) of the following circuits. Assume $\lambda \neq 0$ and $\gamma \neq 0$.







Good luck