EECE488 Analog CMOS Integrated Circuit Design
Assignment 1
Due: Thursday January 28th, 2010 at 9:30am

1. This question is based on Problem 2.13 of the text: The transit frequency, f_T, of a MOS transistor is defined as the frequency at which the small-signal current gain of the transistor is equal to unity (while the source and drain terminals are held at ac ground).

(a) Show that:

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})}$$

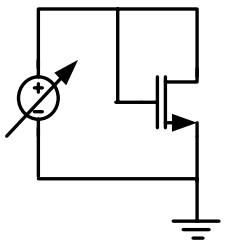
(b) Using square-law characteristics show that for an NMOS of size (W/L) we have

$$f_T \approx \frac{3\mu_n V_{eff}}{4\pi L^2}$$

This relation shows the dependence of speed of operation to the technology feature size and to the supply voltage.

2. (a) Using long-channel MOS equations find the expression for g_m/I_D when the MOS transistor is operating in its active region.

(b) Use HSPICE to simulate the following circuit and plot g_m/I_D versus V_{eff} for an NMOS transistor with W=10.5μm and L=0.35μm when V_{eff} varies between -300mV to 300mV.



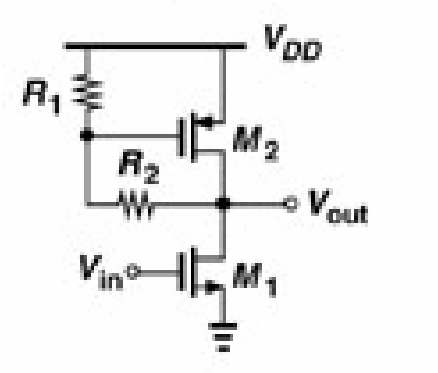
(c) Is there any discrepancy between the simulation result of part (b) and the result expected from the expression in part (a). If yes, briefly explain why?

(d) Repeat part (b) for an NMOS with L=0.7μm.

(e) Repeat part (b) for a PMOS transistor. Note that you need to use a diode-connected PMOS (a PMOS with its gate and drain connected together and source connected to V_{DD}). Compare the results with those of part (b).

3. For the following circuit use HSPICE to sketch Vout versus Vin as Vin varies from 0 to V_{DD}. Identify the important segments (and transition points between the segments) of the curve and the corresponding regions of operation of transistors M_1 and M_2 (e.g., cut-off, linear, or active) for each segment of the curve.

Assume L=0.35μm, $(W/L)_{NMOS}$ = 40, $(W/L)_{PMOS}$ = 30, V_{DD}=3.3V, and R_1=R_2=10kΩ.



Good luck!