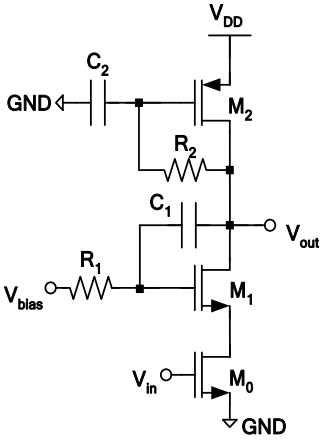
EECE488 Analog CMOS Integrated Circuit Design
Assignment 2
Due: Tuesday February 28th, 2013 at 9:30am

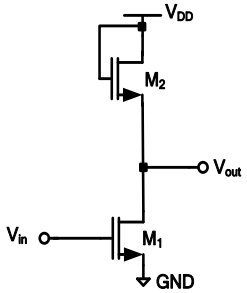
1. Calculate the gain of the following circuit (i.e., provide an expression of the gain in terms of circuit parameters):
a) at very low frequencies
b) at very high frequencies.
In this problem, neglect all other capacitances that are not shown in the circuit and assume $\gamma = 0$ for all three transistors, while $\lambda_0=\lambda_1= 0$ and $\lambda_2 \neq 0$.



2. Design a common-source amplifier with a diode-connected load based on the schematic shown below with the following design specifications:

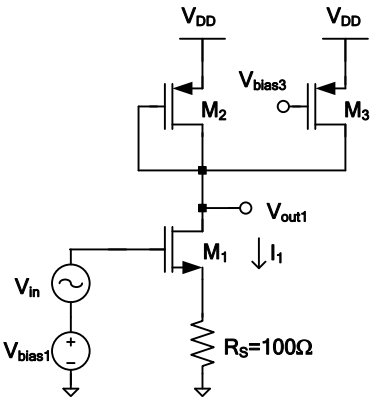
- Transistor M1 is in saturation
- The minimum possible output voltage to keep M1 in saturation is 0.2V
- Total power consumption of the amplifier is 3mW
- Both transistors have L=0.5μm and for transistor M_2 we have W2=1 μm

The technology parameters are:
λ(NMOS) = 0, γ = 0, V_{DD}=3V, V_{TH}(NMOS) = 0.5V, $\mu_n C_{ox}$=1 mA/V^2



Find the following values:
a) DC level of the input, b) DC level of the output, c) width (W_1) of transistor M_1, d) small-signal gain, and e) Maximum output signal swing for a symmetric output signal.

3. In the following circuit assume that all transistors are operating in the saturation region. Also, assume that $\lambda = \gamma = 0$, V_{DD}=1.8V, V_{bias3}=1.15V, $V_{TH(NMOS)}$ = 0.4V and $V_{TH(PMOS)}$ = -0.4V, $\mu_n C_{ox}$=800 μA/V^2 , $(W/L)_1$ = 40, $\mu_p C_{ox}$=400 μA/V^2, $(W/L)_2$ = 40, $(W/L)_3$ = 40, and R_S=100Ω.



a) Find V_{bias1} such that the bias current of M_1 is I_1=1mA.
b) Calculate the small-signal voltage gain $A_{V1}=V_{out1}/V_{in}$.
c) Calculate the small-signal output impedance seen at the output nodeV_{out1}.

Good luck!