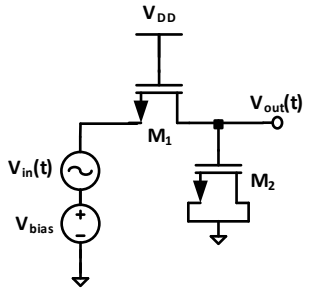
EECE488 Analog CMOS Integrated Circuit Design
Assignment 2
Due: Tuesday October 15th, 2013 at 8:00 am

1. Consider the following circuit:



The technology parameters are:
$\lambda_{(NMOS)}=\lambda_{(PMOS)}=0\ V^{-1}$, $\gamma=0$, $V_{DD}=3.0$ V, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.5$V, $\mu_nC_{ox}=0.1\ mA/V^2$, $\mu_pC_{ox}=0.05\ mA/V^2$, and $C_{ox}= 5\ fF/\mu m^2$.
Assuming the transistor sizes are: $L_1= 0.5\ \mu m$, $L_2= 4\ \mu m$, $W_1= 5\ \mu m$, and $W_2= 20\ \mu m$, and furthermore, $V_{bias}=0.5$ V:
a) What is the region of operation of each transistor**?**
b) If the input signal, V_{in}, is a step function with a small magnitude of 10 mV (i.e., V_{in} abruptly changes from 0 V to 10 mV at time t = 0), what is $V_{out}(t)$ for $t \geq 0$?

2. In the following circuit the DC current of M1 and M2 is 1 mA each and the current of M3 and M4 is 0.5 mA. Assume all transistors are in saturation and the aspect ration of transistors is as follows:
$(W/L)_1 = 125$, $(W/L)_2 = 250$, $(W/L)_3 = 40$, and $(W/L)_4 = 80$.

a) Find g_m of all transistors and r_o of PMOS transistors.
b) Find the voltage gains V_{out1}/V_{in} and V_{out2}/V_{in}

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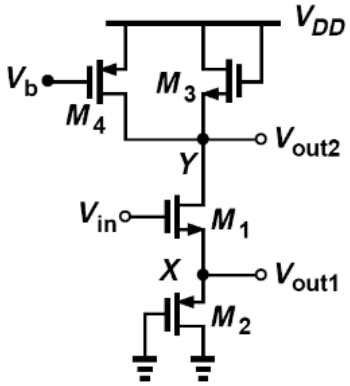

3. In this question, we will estimate the transistor parameters. We will use HSPICE to find these parameters for an NOMS and a PMOS transistor in the 0.35-μm CMOS process used in our class. In all parts of this question, assume that the transistor has a width of W=3.5 μm and length of L=0.35 μm (unless otherwise specified) and V_{DD} = 3.0 V and use two V_{GS} (or V_{SG} in the case of PMOS) of 1 and 2 V. Please make sure to include your HSPICE code.

a) Estimate λ for the NMOS and PMOS transistor (L=0.35 μm)
   Hint: Draw I_D versus V_{DS} for the given values of V_{GS} and from the curve in saturation region estimate λ .
b) Estimate $\mu_n C_{ox}$ and $\mu_p C_{ox}$. Are they equal? What is your intuitive conclusion on the speed of NMOS device versus PMOS?
c) Increase the length to L' = 3×0.35 μm for both NMOS and PMOS and recalculate λ. What will happen to r_o?
d) For L=0.35 μm, use DC – sweep to change V_{BS} (body-source voltage) from 0 to V_{DD} and plot V_{th} versus V_{BS} for V_{GS} (or V_{SG} in the case of PMOS) of 1 and 2 V.
e) Based on your estimated parameters n parts a and b and using the quadratic equation for the current of MOS transistor, calculate the current of the NMOS (W=3.5 μm and L=0.35 μm) for V_{GS} = 1.5 V and V_{DS} = V_{DD} = 3.0 V. Compare your calculated result with that of HSPIC simulation for the same NMOS transistor.