

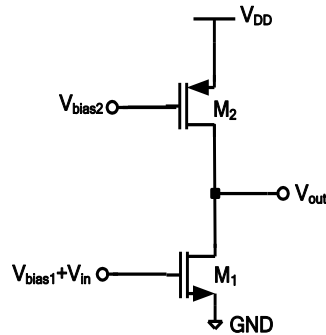
EECE 488: Analog CMOS Integrated Circuit Design
Assignment 2
Due: Thursday, March 1, 2012 at 9:30am

1. Design a common-source amplifier with a current-source load based on the schematic shown below with the following design specifications:

- $V_{DD}=3V$
- Transistor M_1 is in saturation
- The minimum possible output voltage to keep M_1 in saturation is $0.1V$
- The maximum possible output voltage to keep M_2 in saturation is $2.9V$
- Total power consumption of the amplifier is $0.3mW$
- $L=0.4\mu m$ for the transistor

The technology parameters are:

$\lambda_{(NMOS)} = 0.1V^{-1}$, $\lambda_{(PMOS)}=0.2V^{-1}$, $\gamma = 0$, $V_{DD}=3V$, $V_{TH(NMOS)} = 0.5V$, $V_{TH(PMOS)} = -0.6V$
 $\mu_n C_{ox}=1 \text{ mA/V}^2$, $\mu_p C_{ox}=0.25 \text{ mA/V}^2$.



Assuming both transistors are in saturation, find the following values:

(simplifying assumption: only use λ when calculating the output resistance of the transistors and ignore it for DC calculations.)

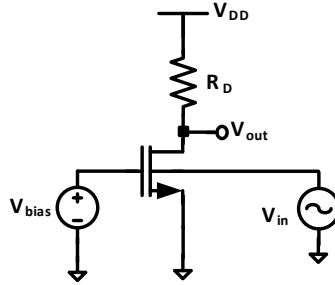
- a) DC level of the input, i.e., V_{bias1}
- b) V_{bias2}
- c) Width (W_1) of transistor M_1
- d) Width (W_2) of transistor M_2
- e) Small-signal gain of the circuit
- f) Is the DC level of the output voltage well-defined?

2. It is possible to use the bulk terminal of a transistor as an input of an amplifier. Consider the single-stage NMOS amplifier shown below. For $V_{\text{bias}}=1.5\text{V}$:

a) What is the region of operation of the transistor?

b) Calculate the small-signal gain ($A_v=V_{\text{out}}/V_{\text{in}}$) of the amplifier. Recall that $g_{\text{mb}}=\eta g_m$.

Assume, $\lambda = 0$, $\eta=0.2$, $V_{\text{TH(NMOS)}}= 0.5\text{V}$, $\mu_n C_{\text{ox}}=100 \mu\text{A/V}^2$, $R_D=1\text{k}\Omega$, $(W/L)_{\text{NMOS}}= 20$, and $V_{\text{DD}}=3\text{V}$. **Note: In this problem, the technology parameters are different from those of Question 1.**



3. Use HSPICE and our 0.35- μm CMOS technology to:

a) Plot the intrinsic gain (i.e., $g_m r_o$) versus V_{DS} for an NMOS transistor of size $W/L=3.5\mu\text{m}/0.35\mu\text{m}$ with a gate-source voltage of $V_{\text{GS}}=V_{\text{th}}+200\text{mV}$.

b) Repeat part a for an NMOS transistor of size $W/L=14\mu\text{m}/1.4\mu\text{m}$.

c) Repeat parts a and b for a PMOS with $V_{\text{SG}}=|V_{\text{th}}|+200\text{mV}$.

Good luck!