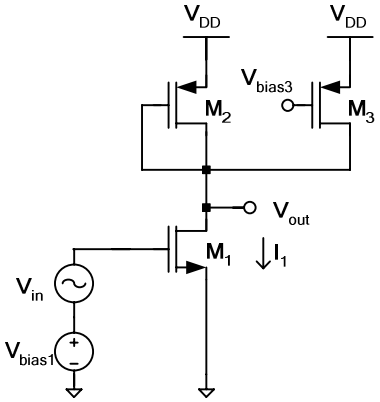
EECE488 Analog CMOS Integrated Circuit Design
Assignment 3
Due: Thursday March 4th, 2010 at 9:30am

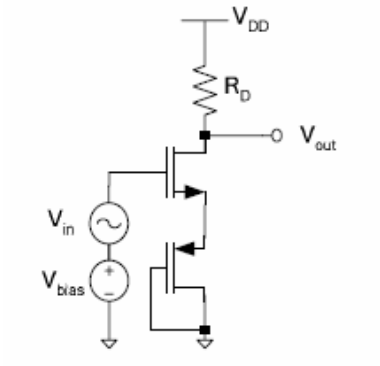
In this assignment, unless otherwise stated, please use the following device parameters:
$\lambda = \gamma = 0$, $V_{TH0(NMOS)}= 0.5V$, $V_{TH0(PMOS)}= -0.6V$, $\mu_nC_{ox} = 200\ \mu A/V^2$, $\mu_pC_{ox}=100\ \mu A/V^2$, and $V_{DD}=3V$.

1. In the following circuit assume that all transistors are operating in the saturation region. Also, assume that $V_{DD}=3V$, $V_{bias3}=1.9V$, $(W/L)_1 = 10$, and $(W/L)_3 = 40$.



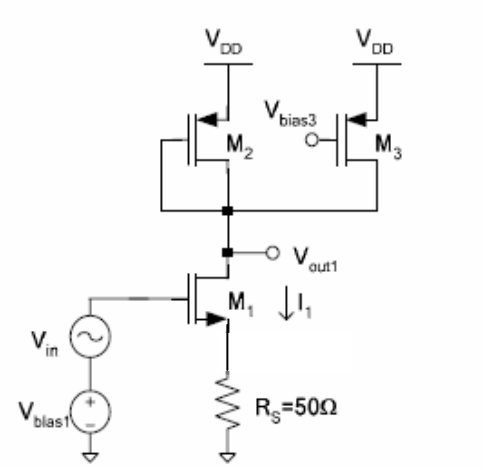
a) Find V_{bias1} such that the bias current of M_1 is $I_1=1mA$.
b) For $I_1=1mA$, find $(W/L)_2$ such that the magnitude of the small-signal gain of the circuit is 2.

2. In the following circuit, assuming that the NMOS transistor is operating in the saturation region and $(W/L)_{NMOS} = 40$ and $(W/L)_{PMOS} = 80$.



a) Find the required V_{bias} for which the dc bias current of the circuit is 1mA.
b) Find R_D such that the magnitude of the small-signal gain of the circuit is 2.
c) Find R_D such that the magnitude of the small-signal gain of the circuit is 20.
d) **Designer X** would argue with you that the value of R_D that you have calculated in part (c) is not a good engineering choice and the gain of your circuit would not be as expected. Please state your reason whether or not you agree with **Designer X**?

3. In the following circuit assume that all transistors are operating in the saturation region and $(W/L)_1 = 40$, $(W/L)_2 = 40$, $(W/L)_3 = 40$, V_{bias3}=1.9V, and R_S=50Ω.



a) Find V_{bias1} such that the bias current of M_1 is I_1=1mA.
b) Calculate the small-signal voltage gain $A_V=V_{out1}/V_{in}$.
c) Calculate the small-signal output impedance seen at the output nodeV_{out1}.

Good luck.