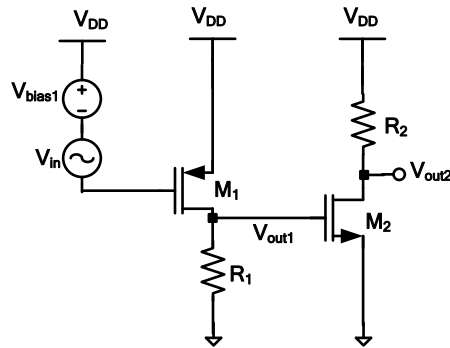


EECE488 Analog CMOS Integrated Circuit Design

Assignment 3

Due: Thursday October 24th, 2013 at 8:00am

1. In the following circuit, assume that $\lambda=\gamma=0$, $V_{DD}=3V$, $V_{TH(NMOS)}=0.5V$, $V_{TH(PMOS)}=-0.5V$, $\mu_n C_{ox}=200 \mu A/V^2$, $\mu_p C_{ox}=100 \mu A/V^2$. Furthermore, assume that V_{in} is a small-signal source and V_{bias1} and the DC level of V_{out1} and V_{out2} are all equal to $V_{DD}/2$. Also, the bias current of M_1 and M_2 are equal.



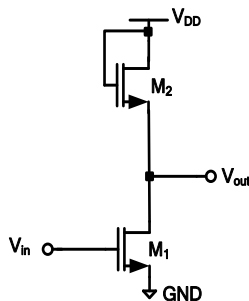
- a) What is the region of operation of M_1 and M_2 .
- b) If the overall power consumption is 3mW, find R_1 , R_2 , $(W/L)_1$ and $(W/L)_2$.
- c) What is the overall gain of the system, i.e., V_{out2}/V_{in} .

2. Design a common-source amplifier with a diode-connected load based on the schematic shown below with the following design specifications:

- Transistor M_1 is in saturation
- The minimum possible output voltage to keep M_1 in saturation is 0.2V
- Total power consumption of the amplifier is 3mW
- Both transistors have $L=0.5\mu m$ and for transistor M_2 we have $W_2=1 \mu m$

The technology parameters are:

$$\lambda(NMOS) = 0, \gamma = 0, V_{DD}=3V, V_{TH(NMOS)} = 0.5V, \mu_n C_{ox}=1 \text{ mA/V}^2$$

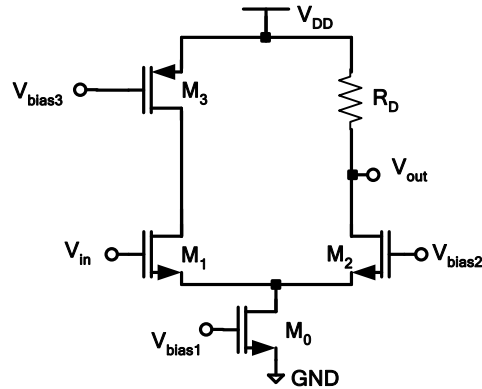


Find the following values:

- a) DC level of the input [5 marks],
- b) DC level of the output [5 marks],
- c) width (W_1) of transistor M_1 [5 marks],
- d) small-signal gain [5 marks]
- e) Maximum output signal swing for a symmetric output signal [5 marks].

3. The input impedance of a common-gate amplifier is typically low. To solve this problem one can use a buffer before the common-gate amplifier. For the following circuit (cascade of a common-drain amplifier and a common-gate amplifier), find the small-signal gain, input and output impedance. Assume that at the frequencies of interest all the device parasitic capacitances can be ignored. Also, assume:

$\lambda_{(NMOS)}=0 \text{ V}^{-1}$, $\lambda_{(PMOS)}=0 \text{ V}^{-1}$, $\gamma=0$, $V_{DD}=1.8 \text{ V}$, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.4 \text{ V}$, $\mu_n C_{ox}=1 \text{ mA/V}^2$, $\mu_p C_{ox}=0.5 \text{ mA/V}^2$, $(W/L)_0 = 32$, $(W/L)_1 = 16$, $(W/L)_2 = 16$, $(W/L)_3 = 32$, $R_D = 1 \text{ k}\Omega$.



Good luck!