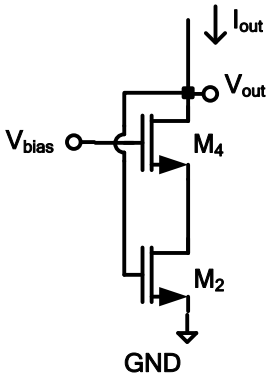
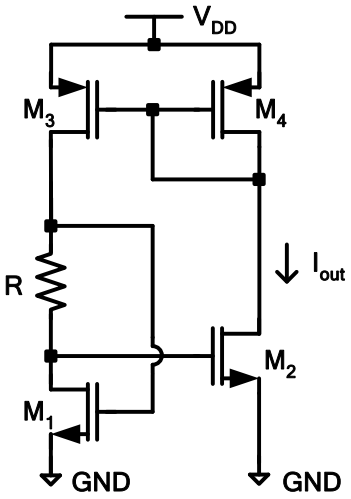
EECE488 Analog CMOS Integrated Circuit Design
Assignment 4
Due: Thursday March 15th, 2012 at 9:30am

2. In the follwing circuit assume that:
$\lambda_{(NMOS)} = 0V^{-1}$, $\gamma = 0$, $V_{DD} = 3$ V, $V_{TH(NMOS)} = 0.5$V, $\mu_n C_{ox}$=1 mA/V^2
Furthermore, assume that I_{out} = 0.5 mA and all transistors have the same size ($\frac{W}{L} = 40$). Find the value of V_{bias} that results in the minimal voltage headroom consumption at node V_{out}. **[10 marks]**



2. Assumibng that all transistors are in saturation, $\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4$, and $\lambda = \gamma = 0$, find an expression for I_{out} in terms of R, transistor parameters (e.g., μ and C_{ox}), and transistor sizes.

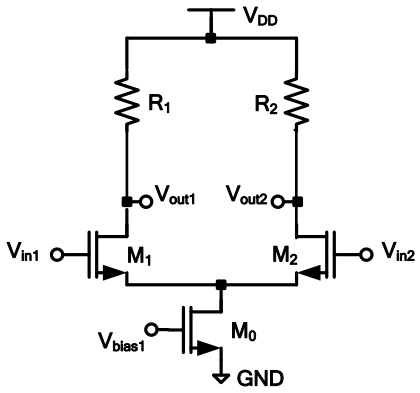


3. Design a symmetric differential amplifier based on the topology shown below with the following design specifications:

- V_{DD}=3.0 V
- Total power consumption of 3.0 mW
- Output DC level of 1.5 V
- Differential gain of 9 V/V
- L=0.4 μm for all devices

Assume that the minimum required voltage at the drain of M_0 to keep it in saturation is 0.2 V.

The technology parameters are:
$\lambda_{(NMOS)}$=0 V^{-1}, $\lambda_{(PMOS)}$=0V^{-1}, γ=0, V_{DD}=3.0 V, $V_{TH(NMOS)}$=|$V_{TH(PMOS)}$|=0.5V, $\mu_n C_{ox}$=1mA/V^2 .



Find V_{bias1}, R_1, R_2, and all the transistor widths (i.e., W_0,W_1, and W_2).

Good luck.