UNIVERSITY OF BRITISH COLUMBIA

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

EECE 488 – Analog CMOS Integrated Circuit Design

Fall 2013

Instructor: Shahriar Mirabbasi (shahriar@ece.ubc.ca), Office: Kaiser 4032, Tel: 604-827-5218
Teaching Assistants: Amir Hossein Masnadi Shirazi (amirms@ece.ubc.ca)

Schedule

Lecture: Tuesdays and Thursdays: 8:00 to 9:30, MCLD 228
Tutorial: Fridays: TBD

Course Outline:

The subject of this course is the analysis and design of analog CMOS integrated circuits. Simple modelling techniques are used to gain a better understanding of the functions of the circuits. Intuitive design methods, quantitative performance measures and practical circuit limitations are emphasized. Circuit performance is predicted by means of both hand calculations and computer simulations. The course contains a review of device modelling, dc and small signal properties of single- and multi-stage amplifiers, followed by the study of biasing circuits, current mirrors, and active loads, differential pairs and operational amplifiers. Next, frequency response characteristics of amplifiers will be examined. If time permits, other topics such as switched-capacitor circuits, data converters, and oscillators will be discussed.

Course Web Page:

Announcements will be posted on the course web page: http://courses.ece.ubc.ca/488/

Recommended Textbook:

Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw Hill, 2001.

Other Useful Reference Material (in no particular ordering):

Tony Chan Carusone, David Johns and Ken Martin, *Analog Integrated Circuit Design*, 2nd Edition, John Wiley & Sons, 2011.
Adel S. Sedra and Kenneth C. Smith, *Microelectronic Circuits*, 6th Edition, Oxford University Press, 2009.
Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th Edition, John Wiley & Sons, 2009.
Phillip E. Allen and Douglas R. Holberg, *CMOS Analog Integrated Circuit Design*, 3rd Edition, Oxford University Press, 2011.
R. Jacob Baker, *CMOS Circuit Design, Layout, and Simulation*, 3rd Edition, Wiley-IEEE Press, 2010.
Journal and conference articles including *IEEE Journal of Solid-State Circuits* and *International Solid-State Circuits Conference*.

Assignments and Project:

There will be a number of assignments and a project associated with this course. Some of the assignments and the project will require the use of HSPICE. They may take a *fair* amount of time, so be sure to start each early.

Late Penalty for Assignments and Projects:

In real-life IC design, fabrication deadlines are hard – if you miss a fabrication deadline, your chip will not be manufactured, your product will not reach market, and your company might go bankrupt. In this course, the late penalty will not be as severe as that, but it is still significant. The late penalty will be *2 dB per weekday (or part of a day)* that the assignment or the project is late.

Mark Breakdown:

Assignments:	10%
Midterm:	15%
Design Project:	25%
Final:	50%