THE UNIVERSITY OF BRITISH COLUMBIA
Department of Electrical and Computer Engineering

EECE 488 – Analog CMOS Integrated Circuit Design
Final Exam
Tuesday April 20th, 2010
Time: 150 minutes

This is an open book exam and calculators are allowed. Please attempt to answer all problems. A blank sheet will not receive any marks!

Good luck!

This examination consists of 12 pages. Please check that you have a complete copy. You may use both sides of each sheet if needed.

#	MAX	GRADE
1	10	
2	10	
3	20	
4	20	
5	20	
TOTAL	80	

Surname First name

Student Number

READ THIS

IMPORTANT NOTE: The announcement "stop writing" will be made at the end of the examination. Anyone writing after this announcement will receive a score of 0. No exceptions, no excuses.

All writings must be on this booklet. The blank sides on the reverse of each page may also be used.

Each candidate should be prepared to produce, upon request, his/her Library/AMS card.

Read and observe the following rules:

No candidate shall be permitted to enter the examination room after the expiration of one-half hour, or to leave during the first half-hour of the examination.

Candidates are not permitted to ask questions of the invigilators, except in cases of supposed errors or ambiguities in examination-questions.

***Caution** - Candidates guilty of any of the following, or similar, dishonest practices shall be immediately dismissed from the examination and shall be liable to disciplinary action:*

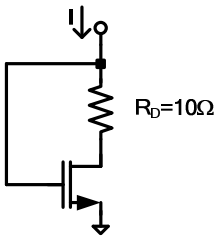
Making use of any books, papers or memoranda, calculators, audio or visual cassette players or other memory aid devices, other than as authorized by the examiners.

Speaking or communicating with other candidates.

Purposely exposing written papers to the view of other candidates.

The plea of accident or forgetfulness shall not be received.

1. Find the maximum bias current I for which the transistor in the following circuit operates in the saturation region. **[10 marks]**
Assume $\lambda = \gamma = 0$, $V_{TH} = 0.5$ V, $\mu_n C_{ox} = 1$ mA/V^2, $(W/L)_{NMOS} = 10$, $R_D = 10\Omega$.



Write your answer in this box

I = _____ mA

2. The magnitude frequency response of a unity-gain closed-loop amplifier shows a peaking of 93% in the vicinity of the gain crossover frequency. What is the phase margin? **[10 marks]**

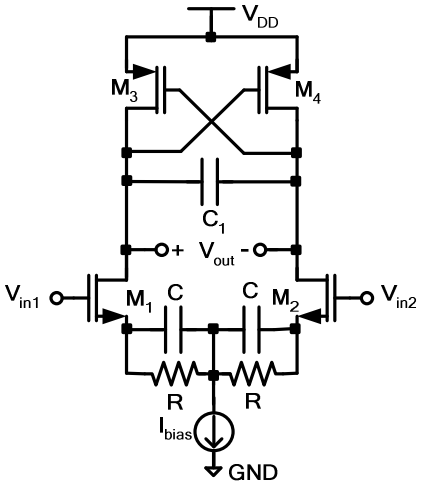
3. Assuming that the following circuit is symmetrical and $\gamma = \lambda = 0$:

i) Find the expression for the small-signal differential voltage gain ($\frac{V_{out}}{V_{in1} - V_{in2}}$) of the circuit at very low frequencies. **[10 marks]**

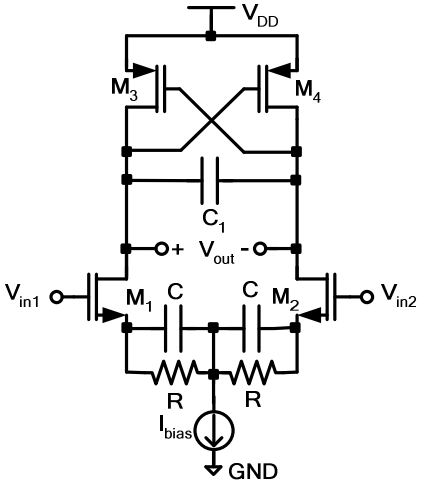
ii) What is the gain of the circuit at very high frequencies? **[5 marks]**

iii) Repeat part (ii) assuming $\lambda \neq 0$. **[5 marks]**

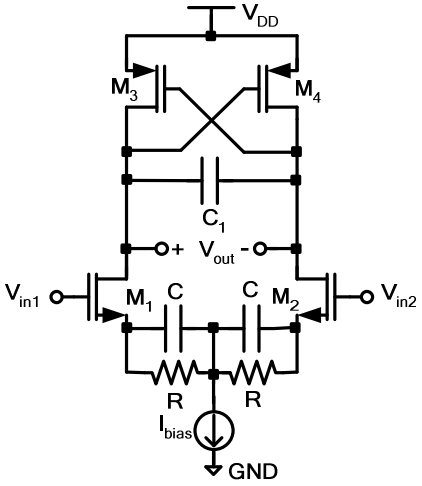
Note: In this question neglect all other capacitances that are not shown in the circuit.



For your convenience the circuit diagram is replicated here:

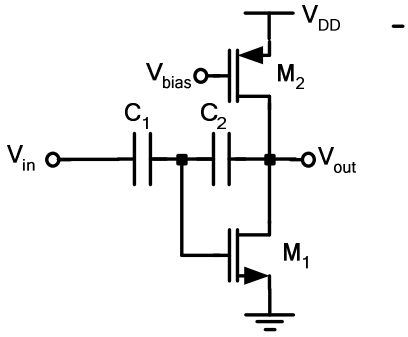


For your convenience the circuit diagram is replicated here:



4. Neglecting all other capacitances and assuming $\lambda = 0$, for the following circuit:

i) Calculate the input impedance. **[8 marks]**
ii) Calculate the output impedance. **[8 marks]**
iii) How would the input impedance change if C_2 is replaced with a resistor. **[4 marks]**



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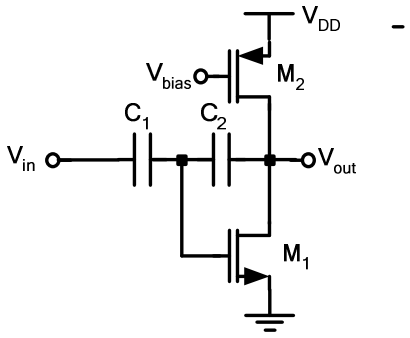


5. Design a two-stage op amp based on the topology shown below with the following design specifications:

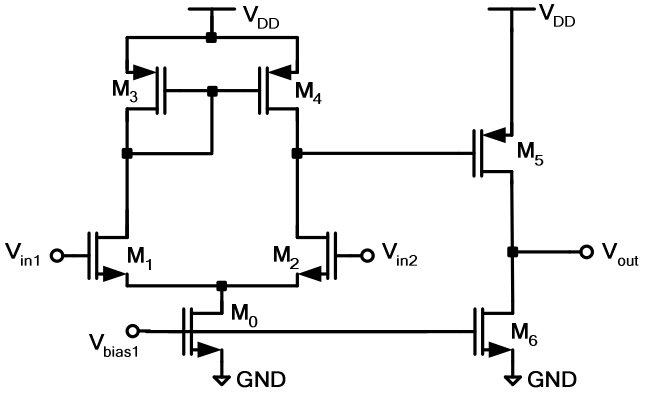
- V_{DD}=3 V
- Total power consumption of 3 mW
- Output swing of 2.6 V
- Total gain of 1000
- L = 0.4μm for all the device

Use the following assumptions for your design

- Allocate equal overdrive voltages to M_5 and M_6
- Assume the bias currents of the first stage and the second stage are equal.
- V_{SG3}=V_{SG5}

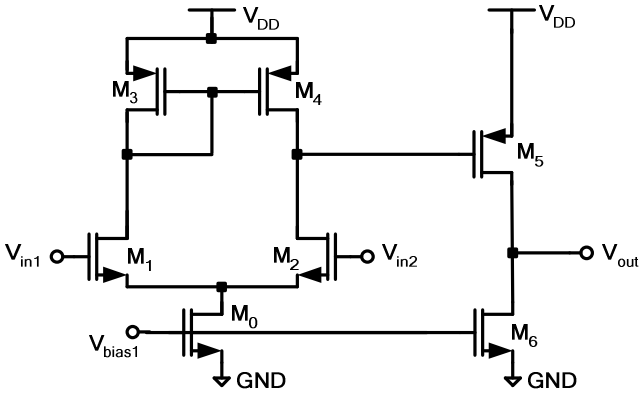
The technology parameters are:
$\lambda_{(NMOS)} = \lambda_{(PMOS)} = 0.1\ V^{-1}$, $\gamma = 0$, $V_{DD} = 3$ V, $V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.5$ V, $\mu_n C_{ox} = 1\ mA/V^2$, $\mu_p C_{ox} = 0.5\ mA/V^2$.

Note: Use the parameter λ only for calculating the r_o of the transistors. **<u>Do not</u>** use λ in any other calculation including your bias currents.



Find V_{bias1}, and all the transistor widths (i.e., W_0,W_1, W_2, W_3, W_4, W_5, W_6). **[20 marks]**

For your convenience the circuit diagram and transistor parameters are replicated here:
$\lambda_{(NMOS)} = \lambda_{(PMOS)} = 0.1\ V^{-1}$, $\gamma = 0$, $V_{DD} = 3$ V, $V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.5$ V, $\mu_n C_{ox} = 1\ mA/V^2$, $\mu_p C_{ox} = 0.5\ mA/V^2$.



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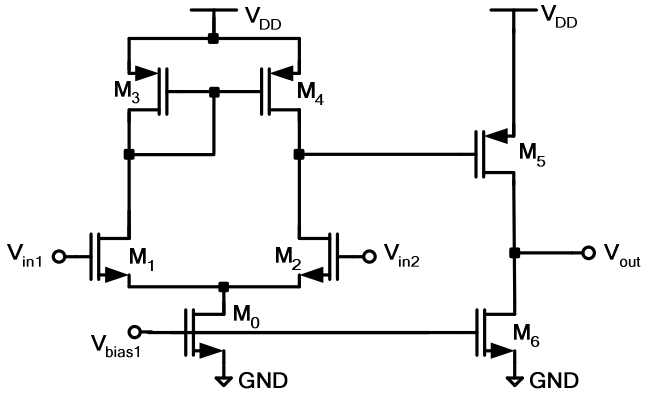

V_{bias1}= _____V, W_0=_____μm, W_1=_____μm, W_2=_____μm

W_3=_____μm, W_4=_____μm, W_5=_____μm, W_6=_____μm,

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