THE UNIVERSITY OF BRITISH COLUMBIA
Department of Electrical and Computer Engineering
EECE 488 – Analog CMOS Integrated Circuit Design
Midterm Exam
Due: Thursday, October 24, 2013 at 8:00 am
Time: 80 minutes

This is an open book exam and calculators are allowed. Please attempt to answer all problems. A blank sheet will not receive any marks! Also, please note that each problem has its own transistor parameters which may be different from other problems.

Good luck!

This examination consists of 8 pages. Please check that you have a complete copy. You may use both sides of each sheet if needed. Please write the final answers to each question in the designated space at the end of each problem.

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Surnames: Solutions

Student Number

IMPORTANT NOTE: The announcement “stop writing” will be made at the end of the examination. Anyone writing after this announcement will receive a score of 0. No exceptions, no excuses.

All writings must be on this booklet. The blank sides on the reverse of each page may also be used.

Each candidate should be prepared to produce, upon request, his/her Library/AMS card.

Read and observe the following rules:

No candidate shall be permitted to enter the examination room after the expiration of one-half hour, or to leave during the first half-hour of the examination.

Candidates are not permitted to ask questions of the invigilators, except in cases of supposed errors or ambiguities in examination-questions

Caution - Candidates guilty of any of the following, or similar, dishonest practices shall be immediately dismissed from the examination and shall be liable to disciplinary action:

Making use of any books, papers or memoranda, calculators, audio or visual cassette players or other memory aid devices, other than as authorized by the examiners.

Speaking or communicating with other candidates.

Purposely exposing written papers to the view of other candidates.

The plea of accident or forgetfulness shall not be received.
1. In the following circuit, assume that $\lambda=\gamma=0$, $V_{DD}=3\,V$, $V_{TH(NMOS)}=0.5\,V$, $V_{TH(PMOS)}=-0.5\,V$, $\mu_nC_ox=200\,\mu A/V^2$, $\mu_pC_ox=100\,\mu A/V^2$. Furthermore, assume that $V_{in}$ is a small-signal source and $V_{bias}=1.5\,V$ and the DC level of $V_{out}$ and $V_{out2}$ are all equal to 0.5 V and 1.5 V, respectively. Also, assume that the bias current of $M_1$ is twice that of $M_2$.

\[ I_1=2I_2 \]

---

a) What is the region of operation of $M_1$ and $M_2$. [2 marks]

b) If the overall power consumption is 3 mW, find $R_1$, $R_2$, $(W/L)_1$ and $(W/L)_2$. [12 marks]

c) What is the overall gain of the system, i.e., $V_{out}/V_{in}$. [6 marks]

\[
\begin{align*}
M_1: \quad & V_{DG1} < |V_{th}| \quad \Rightarrow \quad 0.5 - (3-1.5) < |V_{th}| \\ 
& \quad \Rightarrow \quad -1 < 0.5 \quad \Rightarrow M_1 \text{ in saturation} \\
M_2: \quad & V_{DG2} < |V_{th}| \quad \Rightarrow \quad -0.5 < 0.5 \quad \Rightarrow M_2 \text{ in saturation}
\end{align*}
\]

b) 

\[
P_{dc} = V_{DD} \cdot (I_1 + I_2) \quad \Rightarrow \quad I_1 + I_2 = 1 \, mA
\]

\[
\begin{align*}
\Rightarrow I_1 = 2/3 \, mA \\
I_2 = 1/3 \, mA
\end{align*}
\]

\[
\begin{align*}
V_{out1} = R_1 I_1 \quad \Rightarrow \quad R_1 = \frac{3}{4} \, k\Omega \\
V_{out2} = V_{DD} - R_2 I_2 \quad \Rightarrow \quad R_2 = 4.5 \, k\Omega
\end{align*}
\]

c) 

\[
\begin{align*}
I_{D1} = \frac{1}{2} \mu_nC_{ox} \left( \frac{W}{L} \right)_1 (V_{SG} - V_{th})^2 \quad \Rightarrow \quad \left( \frac{W}{L} \right)_1 = \frac{40}{3} \\
I_{D2} = \frac{1}{2} \mu_pC_{ox} \left( \frac{W}{L} \right)_2 (V_{SG} - V_{th})^2 \quad \Rightarrow \quad \left( \frac{W}{L} \right)_2 = \frac{80}{3}
\end{align*}
\]
For your convenience the circuit diagram and technology parameters are replicated here:

\[\lambda = \gamma = 0, \ V_{DD} = 3\ V, \ V_{TH(NMOS)} = 0.5\ V, \ V_{TH(PMOS)} = -0.5\ V, \ \mu_nC_{ox} = 200 \ \mu A/V^2, \ \mu_pC_{ox} = 100 \ \mu A/V^2.\]

\[C) \ \begin{align*}
    g_{m1} &= \frac{2ID_1}{V_{eff1}} = 2 \cdot \frac{2/3}{1} = 4/3 \ mS  \\
    g_{m2} &= \frac{2ID_2}{V_{eff2}} = 2 \cdot \frac{1/3}{0.5} = 1 \ mS
\end{align*}\]

\[A_V = \frac{V_{out2}}{V_{in}} = \left( \frac{V_{out2}}{V_{out1}} \right) \cdot \left( \frac{V_{out1}}{V_{in}} \right) = \left( g_{m2} \left( \frac{1}{g_{m2} || R_2} \right) \right) \cdot \left( -g_{m1} R_1 \right)\]

\[= -\frac{g_{m1} g_{m2} R_1 R_2}{1 + g_{m2} R_2} = -\frac{6}{1 + 6} = -6/7\]

- \(M_1\) is in \underline{sat.} region. \(R_1 = 0.75\ k\Omega\), \((W/L)_1 = \underline{40/3}\)

- \(M_2\) is in \underline{sat.} region. \(R_2 = 4.5\ k\Omega\), \((W/L)_2 = \underline{80/3}\)

- \(V_{out}/V_{in} = -6/7\)

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2. Design a common-source amplifier with a current source load based on the topology shown below with the following design specifications:
- $V_{DD} = 3$ V
- Total power consumption of 1.5 mW
- Peak to peak output signal swing of 2.5 V
- Absolute value of gain of 40
- $L = 0.4 \, \mu\text{m}$ for all the devices

Use the following assumptions for your design
- The nominal dc level of the output node is 1.5 V

The technology parameters are:
- $\lambda_{(\text{NMOS})} = 0.1 \, \text{V}^{-1}$, $\lambda_{(\text{PMOS})} = 0.1 \, \text{V}^{-1}$, $\gamma = 0$, $V_{TH(NMOS)} = 0.5\, \text{V}$ and $V_{TH(\text{PMOS})} = -0.5\, \text{V}$,
- $\mu_pC_{ox} = 0.2 \, \text{mA}/\text{V}^2$, $\mu_nC_{ox} = 0.1 \, \text{mA}/\text{V}^2$.

Note: Use the parameter $\lambda$ only for calculating the small-signal output resistance ($r_o$) of the transistors. Do not use $\lambda$ in any other calculation including the bias current calculations.

Find $V_{bias}$, DC level of the input, the transistor widths (i.e., $W_1$ and $W_2$), and the gain of the circuit. [20 marks]

- $V_{out\, max}$:
  $$V_{DG} < |V_{th}| \Rightarrow V_{DG\, max} = |V_{th}|$$
  $$\Rightarrow 2.75 - V_{bias} = 0.5$$
  $$\Rightarrow V_{bias} = 2.25$$

- $V_{out\, min}$:
  $$V_{DG_1} < |V_{th}| \Rightarrow V_{DG\, min} = |V_{th}|$$
  $$\Rightarrow V_G = 0.25 = 0.5 \Rightarrow V_G = 0.75\, \text{V}$$

- $I_{D1} = I_{D2} = \frac{1}{2} N_m C_{ox} (\frac{W}{L})_1 (V_{TH})^2 = \frac{1}{2} N_p C_{ox} (\frac{W}{L})_2 (V_{TH})^2$
  $$\Rightarrow (\frac{W}{L})_1 = 32 N_m \Rightarrow (\frac{W}{L})_2 = 160 \Rightarrow W_2 = 64\, \mu\text{m}$$
For your convenience the circuit diagram and technology parameters are replicated here:

The technology parameters are:
\( \lambda_{\text{NMOS}} = 0.1 \text{ V}^{-1} \), \( \lambda_{\text{PMOS}} = 0.1 \text{ V}^{-1} \), \( \gamma = 0 \), \( V_{\text{TH(NMOS)}} = 0.5 \text{V} \) and \( V_{\text{TH(PMOS)}} = -0.5 \text{V} \),
\( \mu_{\text{nCox}} = 0.2 \text{ mA/V}^2 \), \( \mu_{\text{pCox}} = 0.1 \text{ mA/V}^2 \).

Note: Use the parameter \( \lambda \) only for calculating the small-signal output resistance (\( r_o \)) of the transistors. Do not use \( \lambda \) in any other calculation including the bias current calculations.

\[
A_V = \frac{+V_{\text{out}}}{V_{\text{in}}} = -g_{m_1} \left( \frac{r_{o1} \parallel r_{o2}}{r_{o1} \parallel r_{o2}} \right)
\]

\[
= -g_{m_1} \left( \frac{1}{\lambda I_{D1}} \parallel \frac{1}{\lambda I_{D2}} \right)
\Rightarrow

\[
A_V = \frac{-g_{m_1}}{2 \lambda I_{D1}}
\]

\[
\frac{2 I_{D1}}{V_{\text{eff}, 1} \cdot 2 \lambda I_{D1}} = \frac{1}{\lambda V_{\text{eff}, 1}} = -\frac{10}{40}
\]

\[
V_{\text{bias}} = \frac{2.25 \text{ V}}{V_{\text{in, DC}} = \frac{0.75 \text{ V}}{W_1 = 32 \text{ mm}}}
\]

\[
W_2 = 64 \text{ mm}, \frac{V_{\text{out}}}{V_{\text{in}}} = -40
\]

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For your convenience the circuit and the assumptions and circuit parameters are duplicated below:
Assume, $\lambda = \gamma = 0$, $\eta=0.2$, $V_{TH(PMOS)} = -0.6$ V, $\mu pC_{ox} = 100$ $\mu$A/V$^2$, $R_D = 1$ k$\Omega$, $(W/L)_0 = 40$, $(W/L)_1 = (W/L)_2 = 20$, and $V_{DD} = 3$ V.

$$A_{Vd} = \frac{V_{out^+} - V_{out^-}}{V_{in}} = -g_{mb} R_D$$

$$= -2g_m R_D$$

$$= \frac{-2}{\sqrt{2I_{D1}P_{ox}wL}} - R_D$$

$$= -0.4$$

$A_v = -0.4$ (V/V)
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