THE UNIVERSITY OF BRITISH COLUMBIA
Department of Electrical and Computer Engineering
EECE 488 – Analog CMOS Integrated Circuit Design
Take-Home Midterm Exam
Due: Tuseday, March 12, 2013 at 9:30 am

This is an open book exam and calculators are allowed. Please attempt to answer all problems. A blank sheet will not receive any marks! Also, please note that each problem has its own transistor parameters which may be different from other problems.

Good luck!

This examination consists of 12 pages. Please check that you have a complete copy. You may use both sides of each sheet if needed. Please write the final answers to each question in the designated space at the end of each problem.

Solutions

Surname First name

Student Number

#	MAX	GRADE
1	20	
2	20	
3	20	
4	20	
TOTAL	80	

READ THIS

IMPORTANT NOTE: The announcement "stop writing" will be made at the end of the examination. Anyone writing after this announcement will receive a score of 0. No exceptions, no excuses.

All writings must be on this booklet. The blank sides on the reverse of each page may also be used.

Each candidate should be prepared to produce, upon request, his/her Library/AMS card.

Read and observe the following rules:

No candidate shall be permitted to enter the examination room after the expiration of one-half hour, or to leave during the first half-hour of the examination.

Candidates are not permitted to ask questions of the invigilators, except in cases of supposed errors or ambiguities in examination-questions

***Caution** - Candidates guilty of any of the following, or similar, dishonest practices shall be immediately dismissed from the examination and shall be liable to disciplinary action:*

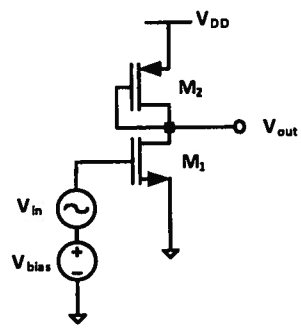
Making use of any books, papers or memoranda, calculators, audio or visual cassette players or other memory aid devices, other than as authorized by the examiners.

Speaking or communicating with other candidates.

Purposely exposing written papers to the view of other candidates.

The plea of accident or forgetfulness shall not be received.

1. Consider the following single-stage amplifier:



The technology parameters are:
$\lambda_{(NMOS)}=\lambda_{(PMOS)}=0\ V^{-1}$, $\gamma=0$, $V_{DD}=3.0$ V, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.5V$, $\mu_n C_{ox}=1\ mA/V^2$, $\mu_p C_{ox}=0.25\ mA/V^2$.

Assuming that both transistors have the same size of: (W/L) =20, M_1 is in saturation and is biased such that its effective voltage is 0.2 V, find:

a) V_{bias} **[4 marks]**.
b) Power consumption of the circuit. **[4 marks]**
c) Small-signal gain of the circuit, i.e., V_{out}/V_{in}. **[8 marks]**
d) What is the maximum output signal swing. **[4 marks]**

a) $V_{eff_1} = V_{GS_1} - V_{th} \rightarrow 0.2V = V_{bias} - 0.5V \rightarrow \boxed{V_{bias} = 0.7V}$

b) $I_{D_1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 V_{eff_1}^2 = \frac{1}{2} \times 1\frac{mA}{V^2} \times 20 \times (0.2)^2 = 0.4\ mA$

$P = VDD \cdot I_{D_1} = 3 \times 0.4 = \boxed{1.2\ mW}$

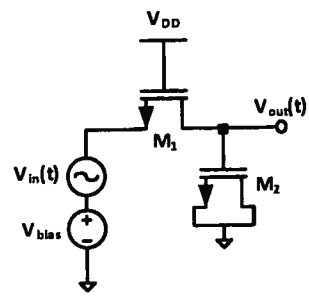
c) $r_o = \infty$, $A_V = -\frac{g_{m_1}}{g_{m_2}} = -\sqrt{\frac{2K_n \cdot \cancel{I_{D1}}}{2K_p \cdot \cancel{I_{D2}}}} = -\sqrt{\frac{\mu_n C_{ox}\cancel{\left(\frac{W}{L}\right)_1}}{\mu_p C_{ox}\cancel{\left(\frac{W}{L}\right)_2}}}$

$A_V = -\sqrt{\frac{\mu_n C_{ox}}{\mu_p C_{ox}}} = -\sqrt{\frac{1}{0.25}} = \boxed{-2\frac{V}{V}}$

d) $\begin{cases} V_{o\,max} = VDD - |V_{th2}| \\ V_{o\,min} = V_{eff_1} \end{cases}$

Max. swing $= VDD - |V_{th2}| - V_{eff_1} = 3 - 0.5 - 0.2 = \boxed{2.3V}$

2. Consider the following circuit:



The technology parameters are:
$\lambda_{(NMOS)}=\lambda_{(PMOS)}=0\ V^{-1}$, $\gamma=0$, $V_{DD}=3.3$ V, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.5$V, $\mu_n C_{ox}=0.1$ mA/V^2, $\mu_p C_{ox}=0.05$ mA/V^2, and $C_{ox}=5$ fF/μm^2.

Assuming the transistor sizes are: $L_1=0.5$ μm, $L_2=4$ μm, $W_1=5$ μm, and $W_2=20$ μm, and furthermore, $V_{bias}=0.8$ V:
a) What is the region of operation of each transistor? **[8 marks]**
b) If the input signal, V_{in}, is a step function with a small magnitude of 10 mV (i.e., V_{in} abruptly changes from 0 V to 10 mV at time t = 0), what is $V_{out}(t)$ for $t \geq 0$? **[12 marks]**
Note: <u>If you need to consider a device capacitance, only take into account the gate capacitance.</u>

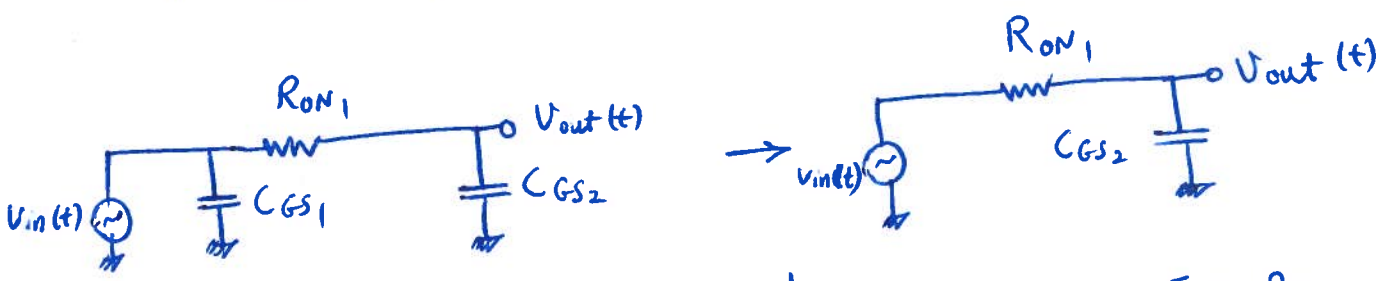
a) $V_{GS_1} = 3.3 - 0.8 = 2.5\ V > V_{th}$, $I_{D_1} = 0$ $\rightarrow$ M_1 is in deep triode region

$V_{DS_1} = 0 \rightarrow V_{G_2} = V_{bias} = 0.8$

$V_{GS_2} = 0.8 > V_{th}$, $I_{D_2} = 0 \rightarrow$ M_2 is in deep triode region.

b)

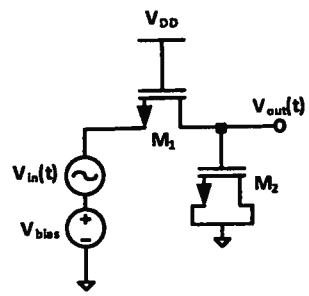
For simplicity, we only consider the gate capacitance (C_{GS}).



$$R_{ON_1} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS_1} - V_{th})} = \frac{1}{0.1\ \frac{mA}{V^2} \times 10 \times (2.5 - 0.5)} = 500\ \Omega$$

$$C_{GS_2} = W_2 L_2 C_{ox} = 20\mu m \times 4\mu m \times \frac{5\ fF}{\mu m^2} = 400\ fF$$

For your convenience the circuit diagram and transistor parameters are replicated here:



The technology parameters are:
$\lambda_{(NMOS)}=\lambda_{(PMOS)}=0\ V^{-1}$, $\gamma=0$, $V_{DD}=3.3$ V, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.5$V, $\mu_n C_{ox}=0.1\ mA/V^2$, $\mu_p C_{ox}=0.025\ mA/V^2$, $C_{ox}=5\ fF/\mu m^2$, $L_1=0.5\ \mu m$, $L_2=4\ \mu m$, $W_1=5\ \mu m$, and $W_2=$ ~~10~~ 20 μm, and $V_{bias}=0.8$ V.

Note: <u>If you need to consider a device capacitance, only take into account the gate capacitance.</u>

$$V_{out}(t) = V_{\infty}\left(1-e^{-\frac{t}{\tau}}\right) + V_{out,DC}$$

$$\tau = R_{ON_1} \cdot C_{GS_2} = 500\ \Omega \times 400\ fF = 200\ ps$$

$$V_{\infty} = 10\ mV = 0.01\ V$$

$$V_{out}(t) = 0.01\left(1-e^{-\frac{t}{200p}}\right) + 0.8\ V$$

M_1 is operating in _____ region and M_2 is operating in _____region.

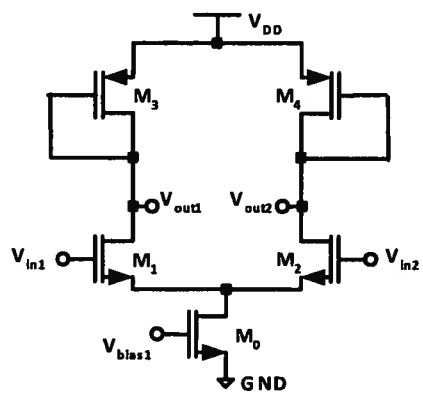
$V_{out}(t)=$

3. Design a differential amplifier based on the topology shown below with the following design specifications:

- V_{DD}=3.0 V
- Total power consumption of 3.0 mW
- Output DC level of 1.5 V
- Differential gain of 40 V/V
- L=0.4 μm for all devices

Assume that the minimum required voltage at the drain of M_0 to keep it in saturation is 0.2 V.

The technology parameters are:
$\lambda_{(NMOS)}=0\ V^{-1}$, $\lambda_{(PMOS)}=0V^{-1}$, $\gamma=0$, $V_{DD}=3.0$ V, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.5V$, $\mu_n C_{ox}=1mA/V^2$, $\mu_p C_{ox}=0.25\ mA/V^2$.



a) Find V_{bias1}, and all the transistor widths (i.e., W_0,W_1, W_2, W_3, and W_4). **[12 marks]**
b) Find the minimum and maximum allowable input common-mode (i.e., input DC) levels **[8 marks]**.

a) $V_{eff_0} = 0.2\ V$

$V_{eff_0} = V_{bias} - V_{th} = 0.2 \rightarrow V_{bias} = 0.2 + 0.5 = \boxed{0.7\ V}$

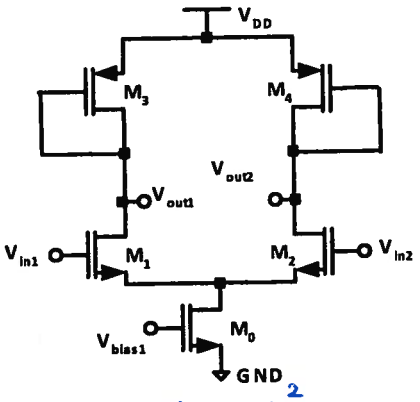
$P = 3\ mW = I_0 \times VDD \rightarrow I_{D0} = \frac{3\ mW}{3\ V} = 1\ mA$

$I_{D0} = 1\ mA = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_0 V_{eff_0}^2 \rightarrow$

$1\ mA = \frac{1}{2} \times 1\ \frac{mA}{V^2} \times \frac{W_0}{0.4}(0.2)^2 \rightarrow \boxed{W_0 = 20\ \mu m}$

$V_{eff_3} = VDD - V_{out}(DC) - |V_{thp}| = 3 - 1.5 - 0.5 = 1\ V$

For your convenience the circuit diagram and transistor parameters are replicated here: $\lambda_{(NMOS)}=0\ V^{-1}$, $\lambda_{(PMOS)}=0V^{-1}$, $\gamma=0$, $V_{DD}=3.0$ V, $V_{TH(NMOS)}=|V_{TH(PMOS)}|=0.5V$, $\mu_n C_{ox}=1mA/V^2$, $\mu_p C_{ox}=0.25\ mA/V^2$.



$$I_{D3} = \frac{I_{D0}}{2} = 0.5\ mA = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_3 V_{eff_3}^2 \rightarrow$$

$$0.5\ mA = \frac{1}{2} \times 0.25\ \frac{mA}{V^2} \times \frac{W_3}{0.4} \times 1^2 \rightarrow \boxed{W_3 = W_4 = 1.6\ \mu m}$$

$$|A_v| = 40 = \frac{g_{m1}}{g_{m3}} = \sqrt{\frac{2\mu_n C_{ox}\left(\frac{W}{L}\right)_1 \cancel{I_{D1}}}{2\mu_p C_{ox}\left(\frac{W}{L}\right)_3 \cancel{I_{D3}}}} = \sqrt{\frac{\mu_n C_{ox} \cdot W_1}{\mu_p C_{ox} \cdot W_3}} \rightarrow$$

$$1600 = \frac{1 \times W_1}{0.25 \times 1.6} \rightarrow \boxed{W_1 = W_2 = 640\ \mu m}$$

b) $V_{in\,min}$ (DC level) $= V_{D_0\,min} + V_{GS_1} = V_{D_0\,min} + V_{eff_1} + V_{th}$

$$I_{D1} = 0.5\ mA = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 V_{eff_1}^2 \rightarrow 0.5\ mA = \frac{1}{2} \times 1\ \frac{mA}{V^2} \times \frac{640}{0.4} V_{eff_1}^2 \rightarrow$$

$$V_{eff_1} = 0.025\ V$$

$$\Rightarrow \boxed{V_{in\,min}\text{ (DC level)} = 0.2 + 0.025 + 0.5 = 0.725\ V}$$

$$V_{GD_1} \leq V_{th} \rightarrow V_{in\,max} - V_{out} \leq V_{th} \rightarrow V_{in\,max} - 1.5 \leq 0.5$$

$$\rightarrow \boxed{V_{in\,max}\text{ (DC level)} = 2\ V}$$

4. In the follwing circuit assume that:
$\lambda_{(NMOS)} = \lambda_{(PMOS)} = 0V^{-1}$, $\gamma = 0$, $V_{DD} = 1.8V$, $I_{bias} = 50\mu A$, $V_{TH(NMOS)} = |V_{TH(PMOS)}| = 0.4V$, $\mu_n C_{ox} = 1\ mA/V^2$, $\mu_p C_{ox} = 0.5\ mA/V^2$.

Furthermore, assume that:

$$\left(\frac{W}{L}\right)_0 = \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = 10$$

$$\left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_6 = \left(\frac{W}{L}\right)_8 = \left(\frac{W}{L}\right)_9 = 20$$

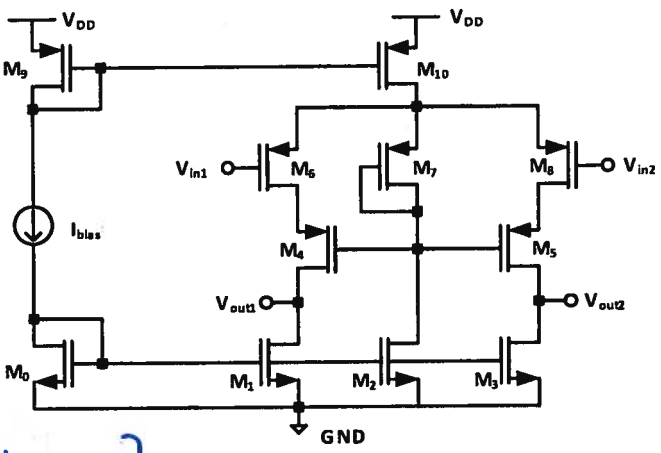
$$\left(\frac{W}{L}\right)_7 = 5, \text{and} \left(\frac{W}{L}\right)_{10} = 60$$

Given that the dc level of the inputs (i.e., input common mode) is 1.2 V:

i) Find the maximum and minimum voltage of V_{out1} and V_{out2} for which all devices stay in saturation. **[12 marks]**

ii) What is the differential output signal swing? **[3 marks]**

iii) Assuming that the circuit is driven by a differential signal, find the magnitude of the differential gain of the circuit, when a resistor of value 10 kΩ is connected between V_{out1} and V_{out2}. **[5 marks]**



$$\left.\begin{array}{l}\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_0 \\ V_{GS_0} = V_{GS_1} = V_{GS_2} = V_{GS_3}\end{array}\right\} \Rightarrow I_{D0} = I_{D1} = I_{D2} = I_{D3} = I_{bias} = 50\,\mu A$$

$$\left.\begin{array}{l}\left(\frac{W}{L}\right)_{10} = 3\left(\frac{W}{L}\right)_9 \\ V_{SG_9} = V_{SG_{10}}\end{array}\right\} \Rightarrow I_{D10} = 3 I_{D9} = 3 I_{bias} = 150\,\mu A$$

$$I_{D7} = I_{D2} = 50\,\mu A$$

$$I_{D6} = I_{D8} = \frac{I_{D10} - I_{D7}}{2} = \frac{150-50}{2} = 50\,\mu A$$

V_{in} (DC-level) $= 1.2\ V$

$$I_{D6} = 50\mu A = \frac{1}{2} \times \frac{1}{2}\frac{mA}{V^2} \times 20 \times V_{eff_6}^2 \rightarrow V_{eff_6} = 0.1\ V$$

$$V_{eff_6} = V_{SG_6} - |V_{th}| \rightarrow 0.1 = V_{S_6} - 1.2 - 0.4 \rightarrow V_{S_6} = V_{S_7} = 1.7\ V$$

$$I_{D7} = 50\mu A = \frac{1}{2} \times \frac{1}{2}\frac{mA}{V^2} \times 5 \times V_{eff_7}^2 \rightarrow V_{eff_7} = 0.2\ V$$

$$V_{eff_7} = V_{SG_7} - |V_{th}| \Rightarrow 0.2 = 1.7 - V_{G_7} - 0.4 \rightarrow V_{G_7} = V_{D_7} = 1.1\ V$$

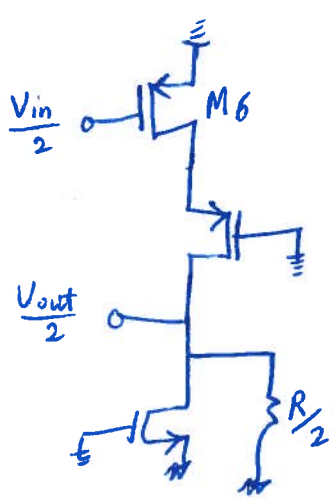
$$I_{D_1} = 50\mu A = \frac{1}{2} \times 1\frac{mA}{V^2} \times 10 \times V_{eff_1}^2 \rightarrow V_{eff_1} = 0.1\ V$$

$$\begin{cases} V_{out\,min} = V_{eff_1} = 0.1\ V \\ V_{DG_4} < |V_{th}| \rightarrow V_{out\,max} - 1.1 < 0.4 \rightarrow V_{out\,max} = 1.5\ V \end{cases}$$

b) Output swing, differential $= 2 \times$ output swing, single-ended

$$= 2 \times (1.5 - 0.1) = 2.8\ V$$

c) Half circuit :



$r_o = \infty$

$$\frac{V_{out}}{2} = -g_{m6} \cdot \frac{V_{in}}{2} \cdot \frac{R}{2} \rightarrow |A_v| = \left|\frac{V_{out}}{V_{in}}\right| = g_{m6} \cdot \frac{R}{2}$$

$$g_{m6} = \sqrt{2 \times \frac{1}{2}\frac{mA}{V^2} \times 20 \times 50\mu A} = 1\frac{mA}{V}$$

$$|A_v| = 1\frac{mA}{V} \times \frac{10K\Omega}{2} = 5$$