1. In the following circuit assume that the bulks of the two NMOS transistors are connected to ground, $l=0$, and $g=0$.

a) What is the region of operation of transistor $M_1$? [10 marks]

b) Does the region of operation of $M_1$ depend on the relative sizing of the transistors. In other word, does it depend on the values $W_1$, $W_2$, $L_1$, and $L_2$. [5 marks]

c) Assume that the $I_{bias}$ and the transistor sizes are chosen such that the drain voltage of $M_1$ is very close to zero. Give an expression for the output resistance of the circuit seen at the drain of $M_2$ in terms of circuit parameters. [5 marks]

\[ V_{D1} = V_{S2}, \quad V_{S2} > V_{th2} \quad (\text{can't be in cut-off}). \]

\[ V_{th2} > V_{th1} \quad \text{due to body effect in } M_2. \]

\[ \therefore V_{D1} > V_{th1} \Rightarrow M_1 \text{ is in triode}. \]

b) No, it does not depend on sizing.

(The reasoning in part (a) does not involve size, only threshold voltage which is independent of size.)
If \( V_y \) is very close to zero, then \( M_1 \) is operating in the deep triode region and can be approximated by a resistance of value:

\[
R_1 = \frac{1}{\mu_n C_\text{ox} \frac{W_1}{L_1} (V_{\text{as}} - V_{\text{th}})}
\]

Can be found if \( I_{\text{bias}} \) is known.

KCL at node "Y":

\[
\frac{V_y}{R_1} = g_{m_2} (V_x - V_y) - g_{m_2} V_y \quad (1)
\]

\[ V_y = I_x R_1 \quad (2) \]

Subst. (2) into (1).

\[
I_x = g_{m_2} V_x - g_{m_2} I_x R_1 - g_{m_2} I_x R_1
\]

\[
I_x (1 + g_{m_2} R_1 + g_{m_2} R_1) = V_x g_{m_2}
\]

\[
\frac{V_x}{I_x} = R_{\text{out}} = \frac{1 + (g_{m_2} + g_{m_2} R_1)}{g_{m_2}}
\]
2. In the following circuit, assuming that the transistor is operating in the saturation region:

a) Find the required $V_{bias}$ for which the dc value of the $V_{out}$ is 1.44V. [10 marks]
b) Is the assumption that the transistor is in the saturation region correct? [4 marks]
c) Find the small-signal gain $V_{out}/V_{sig}$. [6 marks]

Assume $\lambda = 0$, $\gamma = 1V^{1/2}$, $2\Phi_F = 0.64V$, $V_{TH0} = 0.4V$, $\mu_mC_{ox} = 800 \mu A/V^2$, $(W/L)_{NMOS} = 20$, $R_D = R_S = 0.5k\Omega$, and $V_{DD} = 1.8V$.

\[ V_{out} = 1.44V \Rightarrow I_D = \frac{1.8 - 1.44}{R_D} = \frac{1.8 - 1.44}{500} = 720\mu A \]

\[ I_D = \frac{1}{2} \mu_m C_{ox} \frac{V_{eff}^2}{L} \]

\[ 720 \cdot 10^{-6} = \frac{1}{2} \cdot 800 \cdot 10^{-6} \cdot 20 \cdot V_{eff}^2 \]

\[ V_{eff} = 0.09 \Rightarrow V_{eff} = 0.3V. \]

\[ V_X = 720\mu A \cdot R_S = 720\mu A \cdot 500 = 0.36V \]

\[ V_{TH} = V_{TH0} + \gamma \left( \sqrt{2\Phi_F + V_{SD}} - \sqrt{2\Phi_F} \right) \]

\[ = 0.4 + \gamma \left( \sqrt{0.64 + 0.36} - \sqrt{0.64} \right) \]

\[ = 0.4 + \gamma \left( 1 - 0.8 \right) = 0.6V \]

\[ \Rightarrow V_{bias} = V_X + V_{TH} + V_{eff} = 0.36 + 0.6 + 0.3 = 1.26V \]

\[ V_{bias} = 1.26V \]
b.) \( V_D = V_{\text{out}} = 1.44 \, \text{V}, \quad V_G = V_{\text{bias}} = 1.26 \, \text{V} \).

\( V_D > V_G \implies \text{In saturation.} \)

c.)

\[
\begin{align*}
\text{KCL @} \, V_{\text{out}}: \quad & \frac{V_{\text{out}}}{R_D} + g_m (V_{\text{sig}} - V_X) - g_m b V_X = 0, \quad I_{R_S} = -I_{R_D} \implies \frac{V_{\text{out}}}{R_D} = -\frac{V_X}{R_S} \\
V_{\text{out}} & = \frac{1}{R_D} + g_m \left( \frac{V_{\text{sig}} + R_S}{R_D} + g_m b \frac{R_S}{R_D} \right) V_{\text{out}} = 0
\end{align*}
\]

\[
\frac{V_{\text{out}}}{V_{\text{sig}}} = -\frac{4.4 \times 10^{-3}}{\frac{1}{500} + (4.8 \times 10^{-3} + 2.4 \times 10^{-3})}
\]

\[
= -0.522 \frac{V}{V}
\]

\[
\begin{align*}
g_{mb} &= g_m \frac{|V|}{2\sqrt{12|f + V_{ss}|}} \\
g_m &= \mu C_{ox} \frac{w}{L} V_{eff} = 0.0048 \, \text{A/V} \\
g_{mb} &= g_m \cdot \frac{1}{2} = 0.0024 \, \text{A/V}
\end{align*}
\]

Is the assumption that the transistor is in saturation correct? **YES**

\[
\frac{V_{\text{out}}}{V_{\text{sig}}} = -0.522 \frac{V}{V}
\]

Write your answer in this box.
3. Assuming that the following circuit is symmetrical and $\gamma = 0$: and $\lambda \neq 0$:

i) Find the expression for the small-signal differential voltage gain \( \frac{V_{out}}{V_{in1} - V_{in2}} \) of the circuit at very low frequencies. \([15 \text{ marks}]\)

ii) What is the gain of the circuit at very high frequencies? \([5 \text{ marks}]\)

Note: In this question neglect all other capacitances that are not shown in the circuit.

**General Case:**

**Half Circuit:**

\[ g_{m3} V_{as3} = -g_{m3} V_{o1} \]

\[ \frac{V_{o1}}{Z_D} + g_{m1} (V_{in1} - V_s) + \frac{V_{o1} - V_s}{R_o} = 0 \]

\[ \frac{V_s}{Z_s} + g_{m1} (V_s - V_{in1}) + \frac{V_s - V_{o1}}{R_o} = 0 \]

\[ V_s = I_0 Z_s, \ V_o = -I_0 Z_D \rightarrow I_0 = -\frac{V_s}{Z_D} \]

\[ V_s = -\frac{V_o Z_s}{Z_D} \]

**Solved in notes (source degeneration):**

\[ \frac{V_{o1}}{Z_D} + g_{m1} (V_{in1} + \frac{V_{o1} Z_s}{Z_D}) + \frac{V_{o1} Z_s}{Z_D} = 0 \]

\[ \Rightarrow A = \frac{V_{o1}}{V_{in1}} = \frac{-g_{m1} I_0 Z_D}{Z_o (1 + g_{m1} Z_s) + Z_s + Z_o} \]

\[ = \frac{V_{out}}{V_{in1} - V_{in2}} \]
For your convenience the circuit diagram is replicated here:

\[
\begin{align*}
\text{i)} & \quad \text{Low frequencies: } C\ell_{ps} = \text{open circuit.} \\
& \quad Z_0 = -\frac{1}{g_m} \parallel \frac{1}{R_3}, \quad Z_s = R \\
& \Rightarrow A_{LF} = \frac{-g_m \cdot R_0 \left( -\frac{1}{g_m} \parallel \frac{1}{R_3} \right)}{R_0 \left( 1 + g_m \cdot R \right) + R + \left( -\frac{1}{g_m} \parallel \frac{1}{R_3} \right)}
\end{align*}
\]

\[
\begin{align*}
\text{ii)} & \quad \text{Very high frequencies: } C\ell_{ps} = \text{short circuits.} \\
& \quad Z_0 = Z_s = 0 \\
& \Rightarrow A_{HF} = \frac{-g_m \cdot R_0 \cdot 0}{R_0 \left( 1 + g_m \cdot 0 \right) + 0 + 0} = 0
\end{align*}
\]
4. Design a symmetric differential amplifier based on the topology shown below with the following design specifications:
- $V_{DD}=1.8\text{ V}$
- Total power consumption of 1.8 mW
- Output DC level of 0.9V
- Total gain of 5
- $L=0.4\mu m$ for all devices

Assume that the minimum required voltage at the drain of $M_0$ to keep it in saturation is 0.2V.

The technology parameters are:
$\lambda_{(NMOS)}=0 \text{ V}^{-1}$, $\lambda_{(PMOS)}=0\text{ V}^{-1}$, $\gamma=0$, $V_{DD}=1.8\text{ V}$, $V_{TH(NMOS)}=V_{TH(PMOS)}=0.4\text{ V}$, $\mu_nC_{ox}=1\text{ mA/V}^2$, $\mu_pC_{ox}=0.5 \text{ mA/V}^2$.

\[
\begin{array}{c}
\text{V}_{DD} \\
\text{M}_3 \text{ M}_4 \\
\text{V}_{in1} \text{ V}_{in2} \\
\text{V}_{out} \\
\text{V}_{bias} \\
\text{GND} \\
\end{array}
\]

a) Find $V_{bias}$, and all the transistor widths (i.e., $W_0, W_1, W_2, W_3,$ and $W_4$). [14 marks]
b) Find the minimum and maximum allowable input common-mode (input DC) levels [6 marks].

\[ P=1.8\text{ mW} \implies I_{M_0}=1\text{ mA} \]

\[ M_0: \quad \text{Minimum } V_{DD} = 0.2\text{ V} \implies V_{eff_0} = 0.2\text{ V}. \quad (V_{DS} > V_{eff \text{ for saturation}}) \]

\[ V_{bias_1} = V_{eff_0} + V_{TH_0} = 0.2 + 0.4 = 0.6\text{ V} \]

\[ I_{M_0} = \frac{1}{2} \mu_n C_{ox} \left( \frac{W}{L} \right)_0 V_{eff_0}^2 \]

\[ 1 \cdot 10^{-3} \cdot \frac{1}{2} \cdot 10^{-3} \cdot \left( \frac{W}{L} \right)_0 \cdot 0.04 \implies \left( \frac{W}{L} \right)_0 = 50 \implies W_0 = 20\mu m \]

\[ M_{3,4}: \quad \text{Common mode output level is 0.9V.} \]

\[ V_{S_{G3}} = V_{S_{G4}} = 0.9\text{ V} \implies V_{eff_{3,4}} = 0.5\text{ V}. \]

\[ I_{M_{3,4}} = \frac{1}{2} I_{M_0} = \frac{1}{2} \mu_p C_{ox} \left( \frac{W}{L} \right)_{3,4} V_{eff_{3,4}}^2 \]

\[ \frac{1}{2} \cdot 10^{-3} = \frac{1}{2} \cdot 10^{-3} \cdot \left( \frac{W}{L} \right)_{3,4} \cdot \left( \frac{1}{2} \right)^2 \iff \left( \frac{W}{L} \right)_{3,4} = 8 \]

\[ \implies W_{3,4} = 3.2\mu m \]
For your convenience the circuit diagram and transistor parameters are replicated here:

\[ \lambda_{(\text{NMOS})} = 0 \text{V}^{-1}, \lambda_{(\text{PMOS})} = 0 \text{V}^{-1}, \gamma = 0, V_{\text{DD}} = 1.8 \text{V}, V_{\text{TH(NMOS)}} = V_{\text{TH(PMOS)}} = 0.4 \text{V}, \mu_n C_{\text{ox}} = 1 \text{mA/V}^2, \mu_p C_{\text{ox}} = 0.5 \text{mA/V}^2. \]

\[ A = - \frac{g_{m1}}{g_{m3}} \Rightarrow \frac{g_{m1}}{g_{m3}} = 5 \rightarrow \text{Specified gain.} \]

\[ g_{m1} = \sqrt{2 \mu_n C_{\text{ox}} \left( \frac{W}{L} \right)_1 I_{m1}} \]

\[ \frac{g_{m1}}{g_{m3}} = \sqrt{\frac{2 \mu_n C_{\text{ox}} \left( \frac{W}{L} \right)_1 I_{m1}}{2 \mu_p C_{\text{ox}} \left( \frac{W}{L} \right)_3 I_{m3}}} = \sqrt{\frac{\mu_n C_{\text{ox}} \left( \frac{W}{L} \right)_1}{\mu_p C_{\text{ox}} \left( \frac{W}{L} \right)_3}} = \sqrt{\frac{\mu_n C_{\text{ox}} W_1}{\mu_p C_{\text{ox}} W_3}} \]

\[ W_1 = \left( \frac{g_{m1}}{g_{m3}} \right)^2 \frac{\mu_p C_{\text{ox}}}{\mu_n C_{\text{ox}}} W_3 \]

\[ = 25 \cdot \frac{1}{2} \cdot 3.2 \mu \text{m} = 40 \mu \text{m} = W_1 = W_2. \]
For your convenience the circuit diagram and transistor parameters are replicated here: 
\[ \lambda_{(NMOS)}=0 \, \text{V}^{-1}, \lambda_{(PMOS)}=0 \, \text{V}^{-1}, \gamma=0, \ V_{DD}=1.8 \, \text{V}, \ V_{TH(NMOS)}=V_{TH(PMOS)}=0.4 \, \text{V}, \ \mu_{nCox}=1 \, \text{mA/V}^2, \ \mu_{pCox}=0.5 \, \text{mA/V}^2. \]

\[ \begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{circuit_diagram.png}
\end{figure} \]

b.) The minimum input common-mode level is limited by the minimum drain voltage of \( M_0 \) to keep it in saturation.

\[ I_{min} = \frac{1}{2} I_{max} = \frac{1}{2} \mu_{nCox} \left( \frac{W}{L} \right), \ V_{eff} = 0.5 \cdot 10^{-3}. \]

\[ V_{eff} = \frac{0.5 \cdot 10^{-3}}{0.5 \cdot 10^{-3} \cdot \frac{40}{0.4}} = \frac{1}{100} \rightarrow V_{eff} = 0.1 \, \text{V}. \]

\[ V_{cm} = V_{eff} + V_{th} = 0.1 + 0.4 = 0.5 \, \text{V}. \]

\[ \Rightarrow \text{Min } V_{in} = V_{omomin} + V_{cm} = 0.2 + 0.5 = 0.7 \, \text{V}. \]

The maximum input common-mode level is limited by the drain voltage of \( M_{1,2} \), (\( V_{DS} > V_{eff} \) for saturation), or \( V_{DS} < V_{th} \).

\[ V_{DS} < V_{th} \rightarrow V_{in-cm} - V_{D} < V_{th}, \]

\[ V_{in-cm} < V_{th} + V_{D}. \]

\[ \Rightarrow V_{in-cm} < 0.4 + 0.9. \]

\[ \text{Max } V_{in} \leq V_{in-cm} < 1.3 \, \text{V}. \]

\[ V_{bias} = \underline{0.6} \, \text{V}, \ W_0 = \underline{20} \, \mu\text{m}, \ W_1 = \underline{40} \, \mu\text{m}, \ W_2 = \underline{40} \, \mu\text{m}. \]

\[ W_3 = 3.2 \, \mu\text{m}, \ W_4 = 3.2 \, \mu\text{m}, \ V_{in-CM-min} = \underline{0.7} \, \text{V}, \ V_{in-CM-max} = 1.3 \, \text{V}. \]
5. The input impedance of a common-gate amplifier is typically low. To solve this problem one can use a buffer before the common-gate amplifier. For the following circuit (cascade of a common-drain amplifier and a common-gate amplifier), assume that at the frequencies of interest all the device parasitic capacitances can be ignored. Also, assume:
\[ \lambda_{\text{NMOS}} = 0 \text{ V}^{-1}, \quad \lambda_{\text{PMOS}} = 0 \text{ V}^{-1}, \quad V = 0, \quad V_{\text{DD}} = 1.8 \text{ V}, \quad V_{\text{TH(NMOS)}} \approx V_{\text{TH(PMOS)}} = 0.4 \text{ V}, \quad \mu_{\text{n}} C_{\text{ox}} = 1 \text{ mA/}\sqrt{\text{V}}, \quad \mu_{\text{p}} C_{\text{ox}} = 0.5 \text{ mA/}\sqrt{\text{V}}, \quad (W/L)_0 = 32, \quad (W/L)_1 = 16, \quad (W/L)_2 = 16, \quad (W/L)_3 = 32, \quad R_D = 1 \text{ k}\Omega, \quad V_{\text{bias1}} = 0.65 \text{ V}, \quad \text{and} \quad V_{\text{bias2}} = 1.15 \text{ V}.

\begin{center}
\begin{tikzpicture}
  \node (1) at (-1.3,1.3) [circ] {$V_{\text{DD}}$};
  \node (2) at (-2,0) [circ] {$M_0$};
  \node (3) at (0,0) [circ] {$M_1$};
  \node (4) at (2,0) [circ] {$M_2$};
  \node (5) at (3,0) [circ] {$M_3$};
  \node (6) at (1.5,1.5) [circ] {$V_{\text{bias2}}$};
  \node (7) at (-1.5,1.5) [circ] {$V_{\text{bias3}}$};
  \node (8) at (1.5,-1.5) [circ] {$V_{\text{bias1}}$};
  \node (9) at (-1.5,-1.5) [circ] {$V_n$};
  \node (10) at (0,-3) [circ] {$V_{\text{out}}$};
  \node (11) at (0,-3) [circ] {$R_0$};
  \draw (1) -- (2);
  \draw (2) -- (3);
  \draw (3) -- (4);
  \draw (4) -- (5);
  \draw (5) -- (6);
  \draw (5) -- (7);
  \draw (5) -- (8);
  \draw (5) -- (9);
  \draw (5) -- (10);
  \draw (3) -- (11);
\end{tikzpicture}
\end{center}

a) Find the minimum required \( V_{\text{bias2}} \). [5 marks].

b) What is the small-signal voltage gain of the circuit. [10 marks].

c) Calculate (low frequency) input and output impedance of the circuit. [5 marks].

\[
\begin{align*}
V_{\text{gs1}} & = V_{\text{bias1}} - 0.65 \text{ V} \Rightarrow V_{\text{eff1}} = V_{\text{gs1}} - V_{\text{th1}} = 0.65 - 0.4 = 0.25 \text{ V}. \\
I_{D0} & = \frac{1}{2} \mu_{\text{n}} C_{\text{ox}} \left( \frac{W}{L} \right)_0 V_{\text{eff1}}^2 \\
& = \frac{1}{2} \cdot 10^{-3} \cdot 32 \cdot (0.25)^2 = 1 \text{ mA}. \\
V_{\text{gs3}} & = V_{\text{DD}} - V_{\text{bias3}} = 1.8 - 1.15 \text{ V} = 0.65 \text{ V}. \Rightarrow V_{\text{eff3}} = 0.65 - 0.4 = 0.25 \text{ V}. \\
I_{D3} & = \frac{1}{2} \mu_{\text{p}} C_{\text{ox}} \left( \frac{W}{L} \right)_3 V_{\text{eff3}}^2 \\
& = \frac{1}{2} \cdot 10^{-3} \cdot 32 \cdot (0.25)^2 = 0.5 \text{ mA} \\
I_{D3} + I_{D2} & = I_{\infty} \Rightarrow I_{D2} = 0.5 \text{ mA} \\
I_{D2} & = \frac{1}{2} \mu_{\text{n}} C_{\text{ox}} \left( \frac{W}{L} \right)_2 V_{\text{eff2}}^2 \\
& = \frac{1}{2} \cdot 10^{-3} = \frac{1}{2} \cdot 10^{-3} \cdot 16 \cdot V_{\text{eff2}}^2 \Rightarrow V_{\text{eff2}} = 0.25 \text{ V}. \\
V_{\text{bias2}} & \geq V_{\text{DDmin}} + V_{\text{as2}} = V_{\text{th0}} + V_{\text{as2}} = 0.25 + 0.25 + 0.4 = 0.9 \text{ V}. \quad \uparrow \quad V_n
\end{align*}
\]
For your convenience the circuit diagram and transistor parameters are replicated here:

\[ \lambda_{\text{NMOS}} = 0 \quad \text{V}^{-1}, \quad \lambda_{\text{PMOS}} = 0 \quad \text{V}^{-1}, \quad \gamma = 0, \quad V_{\text{DD}} = 1.8 \text{V}, \quad V_{\text{TH(NMOS)}} = |V_{\text{TH(PMOS)}}| = 0.4 \text{V}, \quad \mu_{\text{n}}C_{\text{ox}} = 1 \text{mA/V}^2, \]

\[ \mu_{\text{p}}C_{\text{ox}} = 0.5 \text{ mA/V}^2, \quad (W/L)_0 = 32, \quad (W/L)_1 = 16, \quad (W/L)_2 = 16, \quad (W/L)_3 = 32, \quad R_D = 1k\Omega, \]

\[ V_{\text{bias1}} = 0.65 \text{V}, \quad \text{and} \quad V_{\text{bias2}} = 1.15 \text{V}. \]

\[ \text{Note: This is the technique used on p. 72 (fig 3.33) of the book to simplify the analysis of source followers, but it cannot be used to calculate input impedance.} \]

\[ g_{m1}(V_{in} - V_x) = g_{m2}V_x \rightarrow g_{m1}V_{in} = V_x(g_{m1} + g_{m2}) \]

\[ V_x = \frac{g_{m1}V_{in}}{g_{m1} + g_{m2}} \]

\[ V_{out} = -g_{m2}(0 - V_x) \cdot R_D = g_{m2}V_xR_D \]

\[ = \frac{g_{m2}R_D g_{m1}V_{in}}{g_{m1} + g_{m2}} \]

\[ \Rightarrow A = \frac{V_{out}}{V_{in}} = \frac{g_{m1}g_{m2}R_D}{g_{m1} + g_{m2}} \]

\[ g_{m1} = \sqrt{2I_0u_{\text{th}}(\frac{W}{L})_1} \]

\[ = \sqrt{2 \cdot 10^{-3} \cdot 10^{-3} \cdot 16} = 4 \cdot 10^{-3} \text{A/V} \]

\[ g_{m2} = \sqrt{2I_0u_{\text{th}}(\frac{W}{L})_2} = 4 \cdot 10^{-3} \text{A/V.} \]

\[ A = \frac{4 \cdot 10^{-3} \cdot 4 \cdot 10^{-3} \cdot 10^{-3}}{4 \cdot 10^{-3} + 4 \cdot 10^{-3}} = 2 \frac{V}{V} \]
For your convenience the circuit diagram and transistor parameters are replicated here:
\( \lambda_{(\text{NMOS})} = 0 \) V\(^{-1}\), \( \lambda_{(\text{PMOS})} = 0 \) V\(^{-1}\), \( \gamma = 0 \), \( V_{\text{DD}} = 1.8 \) V, \( V_{\text{TH(NMOS)}} = |V_{\text{TH(PMOS)}}| = 0.4 \) V, \( \mu_n C_{\text{ox}} = 1 \) mA/V\(^2\), \( \mu_p C_{\text{ox}} = 0.5 \) mA/V\(^2\), \( (W/L)_0 = 32 \), \( (W/L)_1 = 16 \), \( (W/L)_2 = 16 \), \( (W/L)_3 = 32 \), \( R_D = 1k\Omega \), \( V_{\text{bias1}} = 0.65 \) V, and \( V_{\text{bias2}} = 1.15 \) V.

\[\text{C.} \quad \text{Low frequency: Gate is open circuit (no gate current).} \]

\[\Rightarrow Z_{in} = \infty. \]

From the small signal model, \( V_{\text{out}} \) does not affect \( I_m \) or \( V_{\text{in}} \) \( \Rightarrow Z_{out} = R_D = 1k\Omega. \)

\[ V_{\text{bias2}} = \begin{array}{c} 0.9 \text{ V} \\ \end{array}, \quad \begin{array}{c} A_v = 2 \text{ V/V} \\ \end{array}, \quad \begin{array}{c} R_{\text{in}} = \infty \text{ } \Omega \\ \end{array}, \quad \begin{array}{c} R_{\text{out}} = 1 \text{ k}\Omega \end{array} \]