EECE 488 Analog CMOS Integrated Circuit Design
Design Project: Opamp Design
Due: Saturday April 20, 2013 at 23:59

The objective of this project is to design a differential input single-ended output CMOS opamp for a specific application where the opamp will be used as a buffer as shown in Figure 1. For this design only NMOS, PMOS transistors, capacitors, and resistors can be used. You are asked to use the 0.35µm CMOS technology for this design. The corresponding model file can be accessed through:

/ubc/ece/home/courses/eece488/hspice/cmosp35/mm0355v.l

The opamp should have PMOS differential input transistors and should consist of single folded-cascode stage. Ideal sources **cannot** be used **except** for V_{DD} and V_{SS} (i.e., ideal sources cannot be used to generate bias currents or voltages, however, it is suggested that in the first pass of your design, you use ideal bias current sources and then once you met the specifications replace the bias sources with an appropriate circuit). The unity gain buffer of Figure 1 is intended for either input step signals or sinusoidal signals with frequencies less than 5 MHz (Note that you are asked to over design for the unity gain frequency of the opamp). The design specifications are summarized in Table 1.

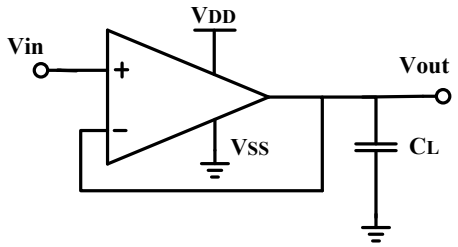

Figure 1. Opamp in unity-gain feedback (i.e., unity buffer)

Table 1. Design Specifications

Process	0.35µm CMOS
V_{DD}	3.3 V
V_{SS}	0 V
Load	1 pF
ADM0 (low-frequency open-loop small-signal gain)	≥ 70 dB
ACM0 (low-frequency open-loop small-signal common-mode gain)	≤ -20 dB
Phase margin	≥ 45°
Unity gain frequency	≥ 20 MHz
Slew rate	≥ 10 V/µs
Differential input transistors type	PMOS
Nominal input and output common-mode voltage	1.65 V
Output voltage swing (peak to peak)	≥ 2 V
Output voltage swing (symmetrical)	≥ 1.4 V
Total power consumption	≤ 250 µW

In your report, include the transient output responses for four different input steps with amplitudes of 0.1V, 1V, -0.1V, and -1V. Measure and report the initial rising/falling slopes of

the output and also the 1% settling times (this is the time required for the output to reach within 1% of its final value).

Bonus:

Design your opamp such that the specifications are met under a ±10% variation of the supply voltage.

Suggestion:

You are free to choose any appropriate structure for the implementation of the opamp. A potential solution is shown in Figure 2. Please note that if you decide to use this circuit, you should replace the ideal current source with a real circuit (one solution is to replace the current source with a resistor, however, you could use more elaborate circuits).

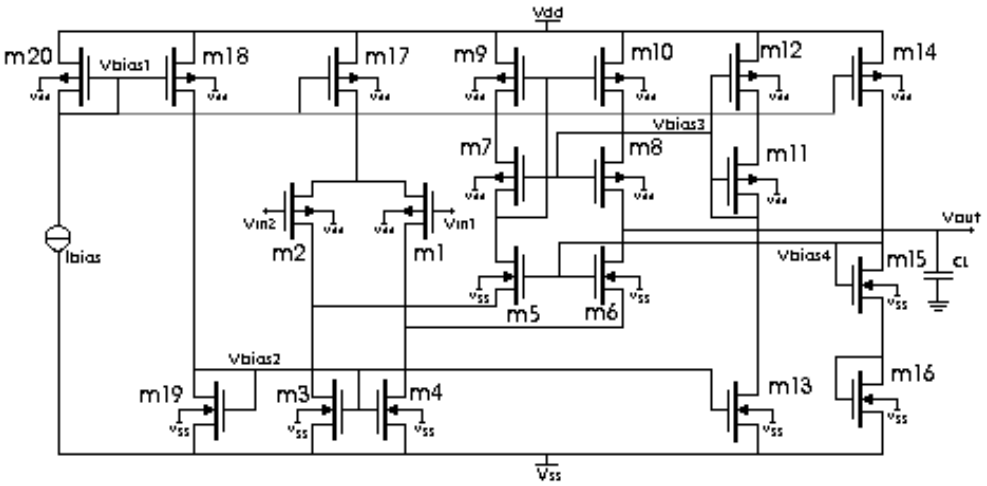

Figure 2. A Folded-Cascode operational amplifier with biasing circuitry

To submit your assignment report and the SPICE code of your design, please follow these steps:

1. Use the following command to create the appropriate directory in your home directory:
mkdir ~/eece488/project
2. Put your SPICE file and any other relevant files such as your assignment report in this directory.
3. Use the following command to handin your project:
handin eece488 project
4. You need to handin at least your spice code and a document which includes your name, student number, a table summarizing the performance results of your opamp, summary of your hand calculations and a brief description of your design approach, required plots including the bode plot of open-loop transfer function on which achieved phase margin and low frequency gain are annotated, bode plot of closed-loop system on which the 3dB frequency of the system is indicated, and any comments and conclusions. Please also include the schematic of your design with transistor sizes and bias currents indicated on the schematic beside each transistor (component values should be indicated beside each component).
5. Any other supporting document(s) or graph(s) that you would like to hand in should be placed in this directory.

Good luck!