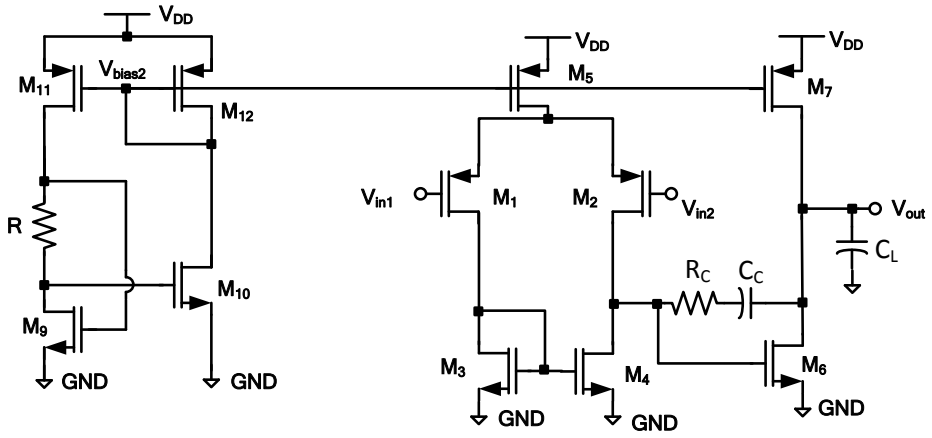
EECE 488 Analog CMOS Integrated Circuit Design
Design Project: Opamp Design
Due: Monday December 16th, 2013, by 11:59pm

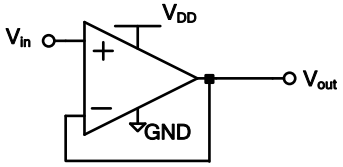
Design and simulate (using HSPICE) a two-stage operational amplifier based on the following topology in the 0.35-µm CMOS process that we have used in our course.



The Design specifications are summarized in the following table:

V_{DD}	3.3 V
GND	0 V
Bias current of M_{12}	100 µA
C_L	2 pF
Nominal input common-mode (input DC level)	1.65 V
Nominal output common-mode (output DC-level)	1.65 ± 0.1 V
Overall power consumption (including bias circuit)	≤ 8 mW
Output peak-to-peak Swing	1.5 V
Low-frequency differential to single-ended gain	≥ 58 dB
Unity gain frequency	≥ 620 MHz
Phase Margin	≥ 60°
Slew rate	≥ 10 V/µs
Maximum length of transistors	$5\times L_{min}$

Assume $W_{11}=W_{12}$ and $W_{10}=4\times W_9$ and all transistors in the bias circuit have the same length. In your design use transistor lengths that are integer multiple of L_{min}. Also, try to use W/Ls that are integer values. After designing the opamp, use it in a closed-loop unity gain configuration shown below. The load capacitance of the opamp is not explicitly shown in the figure, however it is connected between V_{out} and ground. Plot the frequency response of this unity gain structure as well as the transient response for four different input steps that start from 1.65 V with amplitudes of 0.1 V, 1 V, –0.1 V, and –1 V. Measure and report the initial rising/falling slopes of the output and also the 10 to 90% settling time (that is, the time required for the output to reach from 10% to 90% of its final value).



For calculating the output swing use **.measure** command in HSPICE. To submit your project report and the HSPICE code of your design, please follow these steps:

1. Use the following command to create the appropriate directory in your home directrory:
   mkdir ~/eece488/project

2. Put your SPICE file and any other relevant file such as your assignment report in this directory.
3. Use the following command to handin your project: **handin eece488 project**
4. You need to handin at least your HSPICE code and a document which includes your name, student number, a table summarizing the performance results of your opamp, summary of your hand calculations and a brief description of your design approach, required plots including the bode plot of open-loop transfer function on which achieved phase margin and low-frequency gain are annotated, bode plot of closed-loop system on which the 3-dB frequency of the system is indicated, and the step responses, and any comments and conclusions. Please also include the schematic of your design with transistor sizes and component values indicated on the schematic (transistor sizes and component values should be indicated beside each transistor and component, respectively).
5. Any other supporting document(s) or graph(s) that you would like to hand in should be placed in this directory.

Good luck!