1. Design a common-source amplifier with a resistive load based on the schematic shown below with the following design specifications:

- $V_{DD}=1.8V$
- Transistor $M_1$ is in saturation
- The minimum possible output voltage to keep $M_1$ in saturation is $0.2V$
- Total power consumption of the amplifier is $0.9$ mW
- Absolute value of gain of 10
- $L=0.4\mu$m for the transistor

The technology parameters are:

$\lambda_{(NMOS)}=0$, $\gamma=0$, $V_{DD}=1.8V$, $V_{TEH(NMOS)}=0.4V$, $\mu_C=1$ mA/V$^2$.

Find the following values:
1) DC level of the input (2 marks)
2) Width ($W_1$) of transistor $M_1$ (2 marks)
3) $R_D$ (2 marks)
4) Nominal dc level (bias level) of the output node (2 marks)
5) Maximum output signal swing for a symmetric output signal (2 marks)

1) The transistor is in saturation as long as $V_{DS} \geq V_{th} - V_{sat}$. We are told that the transistor leaves saturation when $V_{os}$ falls below $0.2V$.

$$\Rightarrow\quad 0.2 = V_{th} - V_{sat} \Rightarrow V_{sat} = 0.2 + 0.4 = 0.6V$$

and $V_{pep} = 0.2V$. 
2.) From part (1) we know $V_{DD}$, and we can find $I_D$ from the specified power consumption:

$$I_D = \frac{1}{2} \frac{W}{L} V_{DD}^2 = \frac{P}{V_{DD}} = \frac{0.9 \text{ mW}}{1.8 \text{ V}} = 0.5 \text{ mA}$$

$$W = \frac{2 L I_D}{\mu n C_\text{ox} V_{DD}^2} = 10 \text{ m\mu m}$$

3.) From the gain and $g_m$ we can find $R_D$:

$$|AV| = g_m R_D = 10 \quad , \quad g_m = \frac{W}{L} \frac{\mu n C_\text{ox}}{V_{eff}} = \frac{2 I_D}{V_{eff}}$$

$$R_D = \frac{10}{g_m} = 2 \text{ K\Omega}$$

4.) From the bias current and $R_D$ we can find the DC level of $V_{out}$:

$$V_{out} = V_{DD} - I_D R_D = 1.8 - (0.5 \times 10^{-3} \times 2 \times 10^3)$$

$$= 1.8 - 1 = 0.8 \text{ V}$$

5.) The output signal cannot swing above $V_{DD}$ or below the specified 0.2V.

$$1.8 \text{ V} \uparrow \quad \text{1V}$$

$$0.8 \text{ V} \uparrow \quad \text{0.6V.} \Rightarrow \text{Maximum symmetric output swing is } \pm 0.6 \text{ V}$$