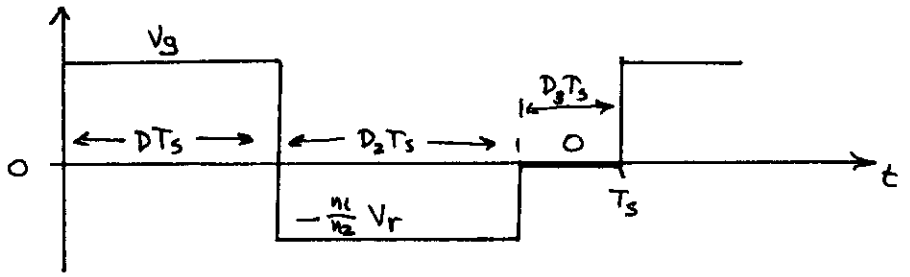
Problem 6.9

a) Transformer voltage waveform, referred to primary winding:



Volt-second balance: $DV_g - \frac{n_1}{n_2} D_2 V_r = 0$

the minimum V_r leads to $D_2 = 1-D$:

$$DV_g - \frac{n_1}{n_2}(1-D)V_{r,min} = 0$$

$$\Rightarrow V_{r,min} = \frac{D}{1-D}\frac{n_2}{n_1}V_g$$

note that max D can lie anywhere within the range $0 \le D < 1$, and is not restricted to $0 \le D < \frac{1}{2}$

b) Peak transistor voltage (not counting ringing and spikes induced by transformer leakage inductance) occurs during reset interval $DT_s < t < (D+D_2)T_s$, and is equal to V_g plus the reflected V_r:

$$\max v_{DS} = V_g + \frac{n_1}{n_2}V_r = \frac{V_g}{1-D}$$

c) now $127 \le V_g \le 380$, $V = 12$, $P = 480W$

Choose turns ratio to minimize total active switch stress

$$S = (\text{worst-case } V_{pk})(\text{worst case } I_{rms})$$

note that worst-case transistor voltage does not necessarily occur at the same operating point as the worst-case rms transistor current.

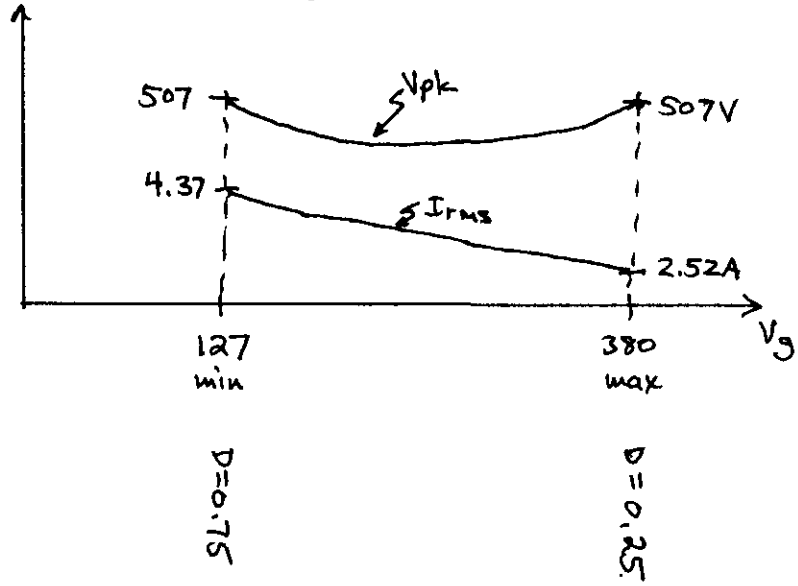
Basic equations:

rms transistor current $I_{rms} = \frac{n_3}{n_1} I_{load} \sqrt{D}$

peak transistor voltage $V_{pk} = \frac{V_g}{1-D}$

with $D = \frac{V}{V_g} \frac{n_1}{n_3}$

<u>Result</u> the choice $\frac{n_3}{n_1} = 0.126$ leads to the following performance:



The total switch stress is $(4.37A)(507V) = 2213\ VA$

d) Compare with conventional design having $n_1 = n_2$ and $V_r = V_g$.

Then worst-case V_{pk} is $2\ max(V_g) = 2 \cdot 380V = 760V$

With this reset scheme, the circuit is limited to $D \leq \frac{1}{2}$.

Choose $\frac{n_3}{n_1}$ so that $D = \frac{1}{2}$ at min V_g (in practice, some additional design margin would be employed):

$$\frac{n_3}{n_1} = \frac{V}{DV_g} = \frac{(12)}{(\frac{1}{2})(127)} = 0.189$$

maximum transistor current occurs at min V_g:

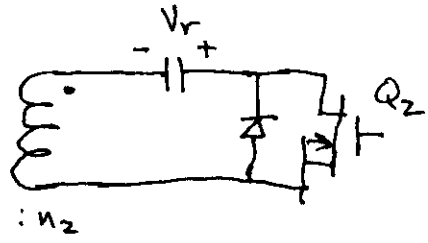
$$I_{rms} = (0.189)(40A)\sqrt{\frac{1}{2}} = 5.35A$$

so the total switch stress is

$$S = (760V)(5.35A) = 4062\ VA$$

which is considerably larger than the value obtained in part (c). The optimal reset scheme allows use of a smaller transistor.

(e) There are many ways to implement the reset circuitry. One way, the "active clamp" circuit:



Q_2 is turned on when Q_1 is off.

The capacitor acts as an unloaded flyback output. The two-quadrant switch prevents DCM.