University of British Columbia

Electrical and Computer Engineering

EECE 493 Power Electronics

Laboratory Handbook (L1A, L1B)

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Contacts:

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1. Scope

The purpose of the EECE493 laboratory project is to individually design, build and test a DC-DC converter, as in Figure 1. You will first manually adjust the duty cycle (open loop driver circuit). Later, you will test with a closed-loop PWM controller, to get constant output voltage with variable input.

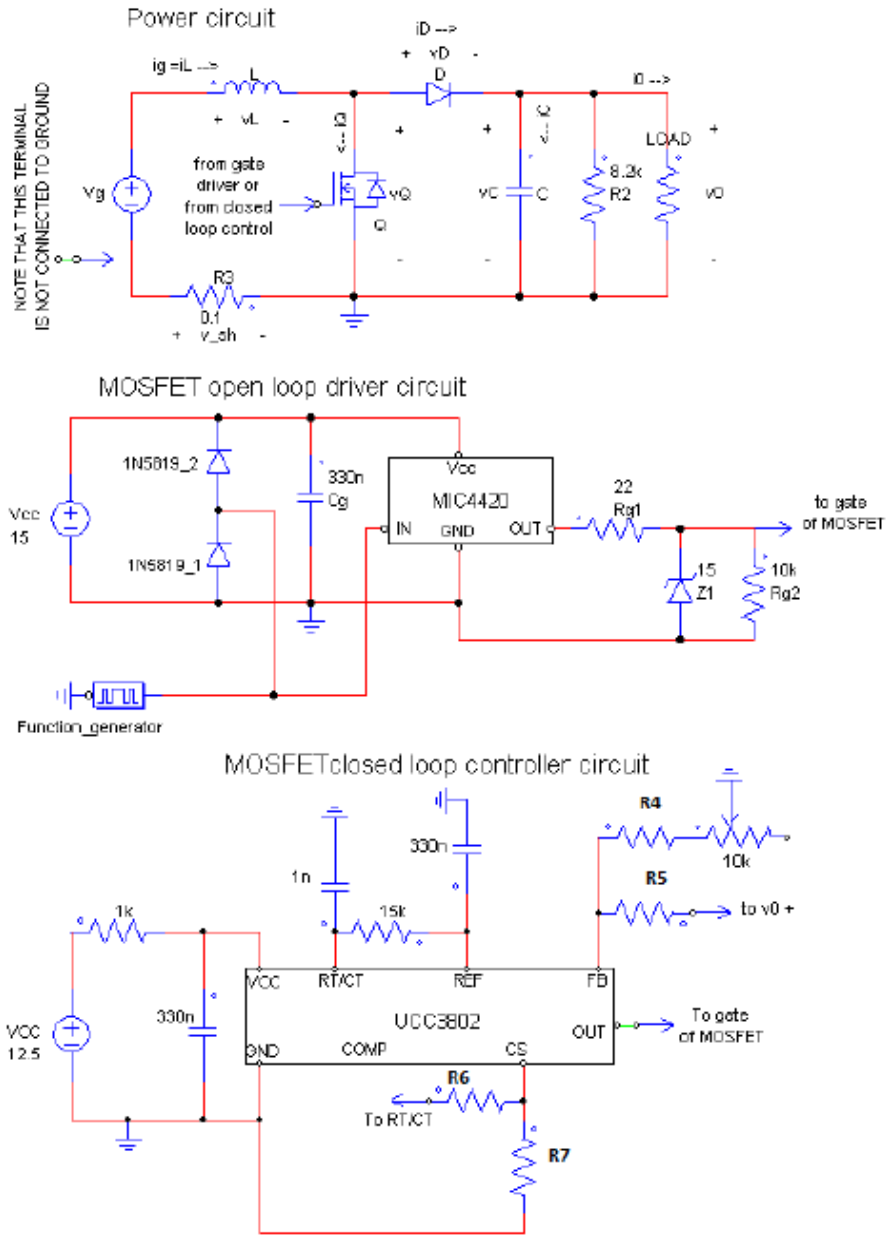

Figure 1. Schematic diagram

$R3=R_{sh}$ is a 0.1 precision shunt resistor used to monitor inductor current with oscilloscope voltage probes (be careful with polarity and ground).

R2 is a pre-load resistor ($R2>>R_{LOAD}$)

MIC4420 is an amplifier, because function generator would not provide enough power to the MOSFET directly.

The load will be an adjustable power resistor externally connected to your circuit.

2. Specifications (Open loop)

Topology: Boost

Input voltage (Vg): + 12 V dc Output

Voltage (Vo): + 48V dc Maximum load

Power: 30W (resistive).

Switching frequency: 40kHz

Maximum input current ripple: ± 10%

Maximum output voltage ripple: ± 0.05%

3. Safety

Read the entire handbook before working with the components provided (check that they are complete) and ask your TA if anything missing or unclear.

Ensure not to reverse the polarity, otherwise, explosion of electrolytic capacitor may occur. Verify the value of the load resistor, over current will overheat components, and may damage semiconductors irreversibly.

Remember that all the channels of the oscilloscope have the same ground, which is connected to the earth ground. Be careful not to make a short-circuit when taking measurements with the oscilloscope, either single channel or simultaneous channels.

4. Schedule

The time scheduled will be only used to build and test your converter and to answer any questions you may have. Therefore, you can work at the scheduled times and/or at any other time; proper access to lab or equipment at other times is your responsibility. Manage your time appropriately in order to have your converter ready for demos not after the due date.

You are expected to provide your own tools, such as pliers, cutters, screwdriver, tape and bread board (optional for preliminary tests). Solder stations are limited; you will need to share them.

Session #	Section A	Section B
1	Oct 3	Oct 4
2	Oct 17	Oct 18
3	Oct 31	Nov 1
4	Nov 14	Nov 15
Demo 1 (open loop) due date	Oct 31	Nov 1
Demo 2 (closed loop) due date	Nov 28	Nov 29

5. Due dates

Four reports must be submitted, drop them in the box outside **Kaiser 3085** not later than **7:00 PM** of the specified date. Late reports may not be accepted unless justified and approved by the instructor. Keep a copy of your first reports as you may need data for subsequent ones.

Report #	Section A	Section B
1	Oct 17	Oct 18
2	Oct 24	Oct 25
3	Nov 7	Nov 8
4	Nov 21	Nov 22

6. Marks breakdown

Report #1: 8% **Report #2: 3%** **Demo #1: 4%**

Report #3: 3% **Report #4: 3%** **Demo #2: 4%**

TOTAL: 25% from your EECE493 mark

7. Report specifications

You are allowed to discuss your results and design problems with other students, but report and solutions must be individual. Plagiarism will be penalized as per UBC policies.

Split your reports in the sections indicated in this handbook, **circle or highlight the required results please.**

Calculations and plots by hand are allowed in Report #1 and Report #4; but they should be clean and legible, otherwise they will be marked as wrong.

You are encouraged to use double sided printing or single sided scrap paper. Coversheet is not encouraged, as long as your name, student number, title and date are at the top of first page.

8. Report #1: Conceptual Analysis and Design

I. Topology selection

According to the specifications, you should select and justify from one of the four following topologies: Buck, boost, buck-boost, Cuk. Show the differences among them.

II. Steady state analysis of the Boost Converter

a) Assuming $|\Delta v_C| << |V_C|$ and $|\Delta i_L| << |I_L|$, please get the analytical expressions or V_O, I_L, $|\Delta v_C|$ and $|\Delta i_L|$. Remember to use small ripple approximation, inductor volt-second balance and capacitor charge balance. Calculate the duty cycle (D) required. Neglect losses.

b) Draw the following waveforms. You should align the plots vertically, so that it's clear what happens with each variable during the states of every switching cycle. It's not necessary to draw to scale, just show clearly the waveform shapes and analytical values.

v_L = inductor voltage

i_L = inductor current (slope)

v_L = capacitor voltage (slope)

i_C = capacitor current

v_Q = transistor voltage

i_Q = transistor current

v_D = diode voltage

i_D = diode current

III. Inductance and Capacitance

a) Calculate the minimum value of inductance L such that your design meets the requirement on the current ripple $|\Delta i_L| < 10\% I_L$

b) Calculate the minimum value of capacitance C such that your design meets the requirement on the voltage ripple $|\Delta v_C| < 0.05\% V_C$

IV. Inductor selection (L)

a) This has been done for you. Assume: L = 450μH. Series resistance = 0.15Ω

V. Capacitance selection (C)

a) Calculate the peak voltage across the capacitor C

b) Calculate the RMS current across the capacitor C and its frequency

c) Select the proper capacitor from http://www.chemi-con.com. Consider all the relevant parameters: voltage, RMS current, frequency. Append the datasheet of your selection, highlighting the relevant parameters

VI. Selection of MOSFET (Q)

a) Calculate the peak MOSFET voltage

b) Calculate the peak MOSFET current

c) Calculate the average MOSFET current

d) Calculate the RMS MOSFET current

e) Select the proper MOSFET (N-channel) from http://www.onsemi.com. Consider all the relevant parameters. Append the datasheet of your selection, highlighting the relevant parameters

f) Estimate the loss on MOSFET due to $R_{DS(ON)}$

VII. Selection of Diode (D)

a) Calculate the peak diode voltage

b) Calculate the peak diode current

c) Calculate the average diode current

d) Calculate the RMS diode current

e) Select the proper diode from http://www.onsemi.com. Remember the switching frequency when selecting the type of diode. Append the datasheet of your selection, highlighting the relevant parameters

VIII. Expected efficiency η

Estimate the following losses at maximum load and nominal output voltage

a) MOSFET loss due to $R_{DS(ON)}$

b) Loss on diode due to voltage drop

c) Loss on inductor due to series resistance

d) Loss on capacitor due to R_C=ESR

e) Calculate the converter efficiency η at that load value, based on the above losses

IX. Steady-state equivalent circuit modeling (DC-transformer model)

a) Develop a steady state equivalent circuit of your converter, based on a DC transformer model. Neglect the capacitor series resistance ESR (aka: RC).

b) Calculate the conversion ratio (M = V0/Vg) analytically, show the expression and plot it against 0-100% duty cycle.

c) Calculate the efficiency (η) analytically, show the expression and plot it against 0-100% duty cycle.

d) How does the duty cycle to get V0=48V change due to losses on this model?

9. Report#2: Simulation of boost converter (open loop control)

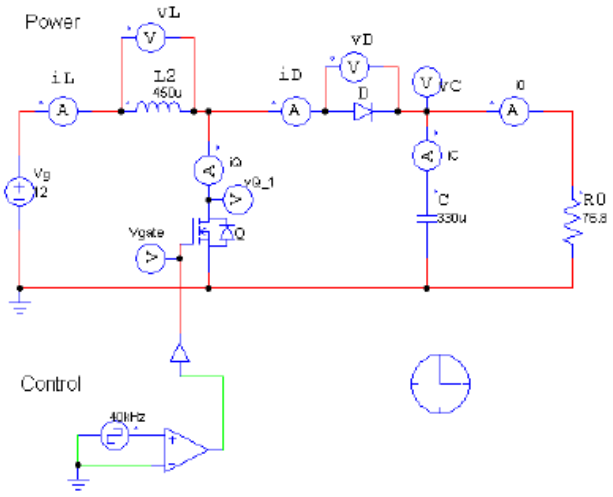

Figure 2. Simulation Schematic in PSIM

Download (if you don't have it already) the PSIM software from http://www.powersimtech.com/download.html. Read the instructions and software help in case you are not familiar with the program.

Reproduce the schematic from Figure 2 of the DC-DC boost converter (preload and shunt resistances are ignored, control circuit is simplified). Set all components as ideal (no resistive losses, no voltage drops)

Set the pulse generator duty cycle to the percentage required for Vg=12V, $V_0 = 48V_{DC}$, as per the topology chosen in your ideal design from Report #1.

Use the following data for simulation control

- Step time: 1E-6 s
- Total time: 2.0000 s
- Print time: 1.9999 s
- Print step: 1

I. Get and show the following waveforms

a) v_L= inductor voltage

b) i_L = inductor current

c) v_L = capacitor voltage

d) i_C = capacitor current

e) v_Q = transistor voltage

f) i_Q = transistor current

g) v_D = diode voltage

h) i_D = diode current

II. Repeat the simulation using print time 0.9999s and total

a) Show the new waveforms obtained for vC and iL only. Explain in one or two sentences why your results are now completely different to your analytical results and to your previous simulation results. Try different times if you need.

III. Repeat the simulation with the original time settings, but:

a) Both ripples |ΔvC|, |ΔiL| must be reduced to half of the previous values, <u>without changing anything on the power circuit</u>. Show and explain what you did.

10. Circuit construction

I. Inductor design and construction

a) You should stack two magnetic cores Magnetics 77071-A7. The core information and design instructions are available on www.mag-inc.com, for reference only.

b) Make 64 turns of winding with magnet wire AWG#20, be careful not to damage the insulation while winding, only remove it in the edges for connection and measurement. If your winding is nicely done, you may have space to wind a few more turns in the single layer, which would be good. Tape helps to keep the winding tight.

c) The total length of wire is about 4.5 meters; from tables $R_{AWG\#20}$=0.033 /m, then the total series resistance is around 0.15 .

d) Use the LC meter available in the lab, to verify and record the real inductance value. Also verify the value of the electrolytic capacitor provided and record it.

II. Circuit

a) The components must be put together and soldered on the provided PC-171 vector board according to the schematics from Figure 1. Verify the pinout of the components in its datasheet. Check resistor values if unsure too.

b) It's suggested, but optional, that you try a layout in your own breadboard first.

c) In order to reduce the inductive loop and avoid gate resonance, the MIC4420 output should not be very far to the MOSFET gate. The 330nF small capacitor should be placed very close or directly over the V_{CC} and GND pins of the driver.

d) The 330nF capacitors in the closed loop controller should also be placed very close to the corresponding terminals of the UCC3802.

e) The D-Q-C loop in the power stage must be as short as possible.

f) Your layout should allow connecting the MOSFET gate either to the output of the gate driver OR to the output of the closed loop controller, so that Demo #1 and Demo #2 can be performed separately. Take out the IC not being used for the test.

g) The inductor core should not be placed very close to the ground or gate control wires, to avoid interference.

h) For testing, you will require two external DC power supplies, one function generator, oscilloscope, multimeter and one variable power resistor as load.

i) It's recommended that you label or use different colors for each of the wires that must be connected from your vector board to the external equipment.

III. Power up and Demo I (open loop, manual duty cycle adjustment)

a) Set the load resistor value to get the 30W output power at 48Vdc. Verify that the negatives of the DC supplies are not connected together, due to shunt resistor.

b) Power up gate driver circuit.

Turn on gate driver DC voltage supply. Ensure all knobs are in zero before. Gradually increase the voltage from 0 to 15V.

c) Power up function generator.

Turn on the function generator. Select square waveform

Use both oscilloscope channels to verify the input and output of MIC4420. Tune function generator until the frequency is 40 kHz and the duty cycle is minimal value for continuous conduction mode (IL>ΔiL).

d) Power up the second DC power supply.

Put a probe to the shunt resistor to monitor input current (iG = iL = - vsh / Rsh)

Gradually increase the input voltage of converter from 0 up to 12V and observe the current change.

Increase the duty cycle (D) slowly from minimal to 80% and observe the change in output voltage while you increase D, to see if your converter works as it is supposed to.

Keeping the same load, do the tests required in Report #3 section.

11. Report #3: Real converter performance (open loop)

I. Duty cycle

a) Set and record the duty cycle (D) value so that $V_0 = 48.0V_{DC}$. Explain why the duty cycle is not the same than in Report #1 or Report #2.

II. Waveforms

a) Keep V_0 = 48.0VDC. Record the oscilloscope plot, or draw manually, with reasonable detail, the waveforms of the transistor voltage v_Q, output voltage v_0 and inductor current i_L. Tune the x-axis scale so that you observe the switching cycles, and the y-axis scale so that you observe the ripples clearly, and not the switching noise peaks. Are those waveforms as expected? Why?

b) Measure the actual capacitor voltage ripple |DvC| and inductor current ripple |ΔiL|, as a percentage of V_C and I_L. Did you meet the specifications?

III. Conversion Ratio

a) Set D at 75%. Change the input DC voltage from 3 to 12VDC in 1V steps. Record the output DC voltage V_0 for each input. Plot V_0 vs V_g and get the conversion ratio (M) at that duty cycle (a linear curve fit is helpful).

IV. Efficiency

a) Keep input voltage at 12V. Vary the duty cycle from minimum to 80%, in 5% steps. Get the input and output DC voltages and currents, for each duty cycle (D). Calculate the conversion ratio (M) and efficiency (h). Plot the curves: M vs D, vs D; and superimpose the plots calculated in the DC transformer model of Report #1. Justify the differences.

12. Report #4: Dynamic analysis (linearization)

I. Transfer functions around the nominal operating point

For the nominal operating point: V_g = 12V, V_0=48V, P_0=48W; and assuming ideal components ($R_{dsON} = R_L = R_C = 0$), derive the following transfer functions. This part does not require your experimental results, only your ideal design data is used.

- Converter control to output transfer function
- Converter line to output transfer function
- Converter output impedance

Draw or print the Bode Plots for each of the transfer functions from above. Make comments highlighting any relevant points in the plots, as per the material covered in EECE493 lectures.

II. Closed loop simulation

The object of this part is to design a closed-loop PWM controller for the Boost converter. To do this, you should first obtain a closed-loop gain and study the effects of disturbances in load and input voltage on output voltage. Then design a *PID* controller, which modifies the closed-loop results. Follow steps below:

No compensation:

Using figure 9.4 of the textbook, transfer functions obtained in part I, assuming no compensator in the loop and unit sensor gain (Gc(s)=H(s)=1), build a model in Matlab/Simulink.

a) Show the effect of +20% step change in load current on output voltage.
b) Show the effect of +10% step change in input voltage source on output voltage.
c) Show the effect of injection of a 1v 120Hz sinusoidal voltage source (harmonic content) to the input dc voltage source (Vg) on the output voltage.

***PID* compensator:**

Read section 9.5 of the textbook. Repeat same design procedure with (crossover frequency=2 kHz and Phase margin=52) and find appropriate P, I and D values for the compensator.

Draw or print bode plots for your new closed loop system for:

- Converter line to output transfer function

- Converter output impedance

Repeat parts a), b) and c) and show the effect of compensator on closed-loop performance.

Describe the design steps and provide related figures and numbers to justify the modifications.

You can also use SISOTOOL in Simulink to find desired P, D and I values automatically. (This part is not mandatory but can help you to understand the linear controller design steps)