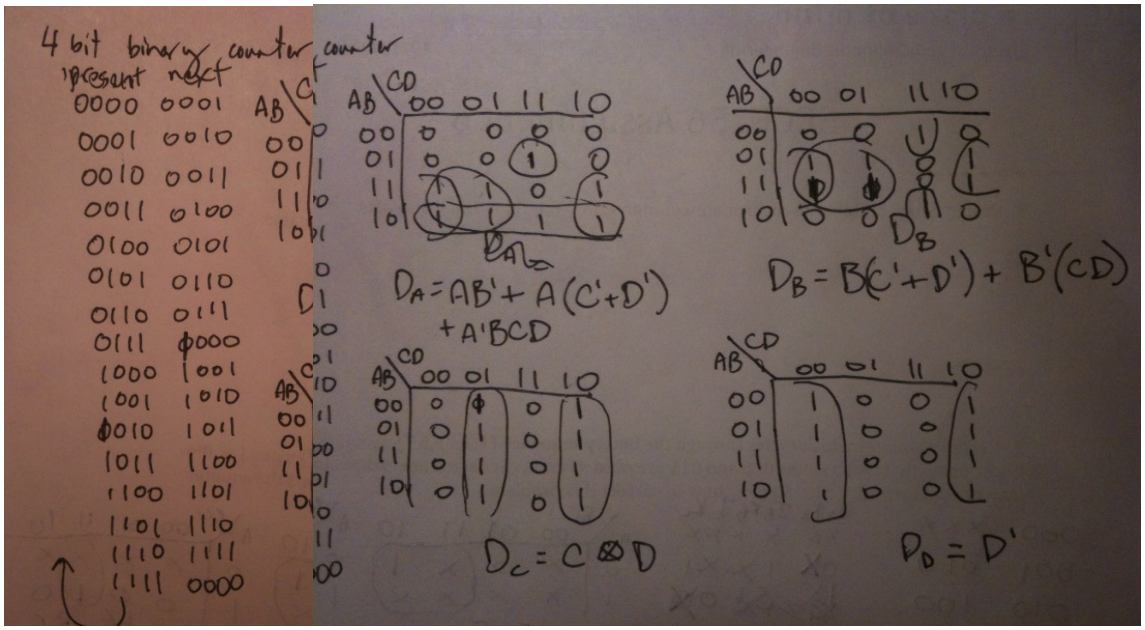
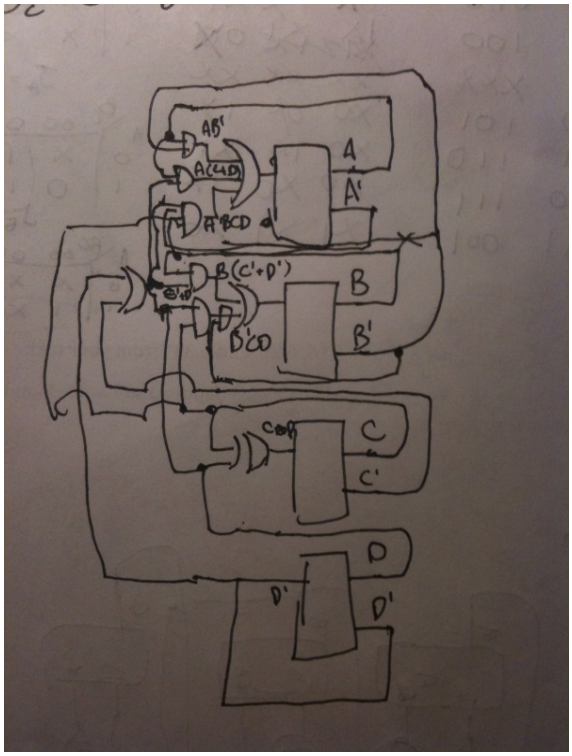
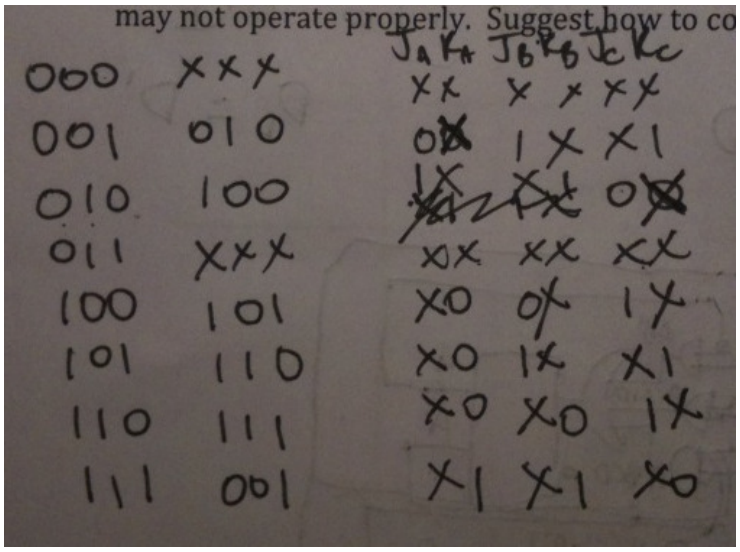
EECE256 Assignment 6

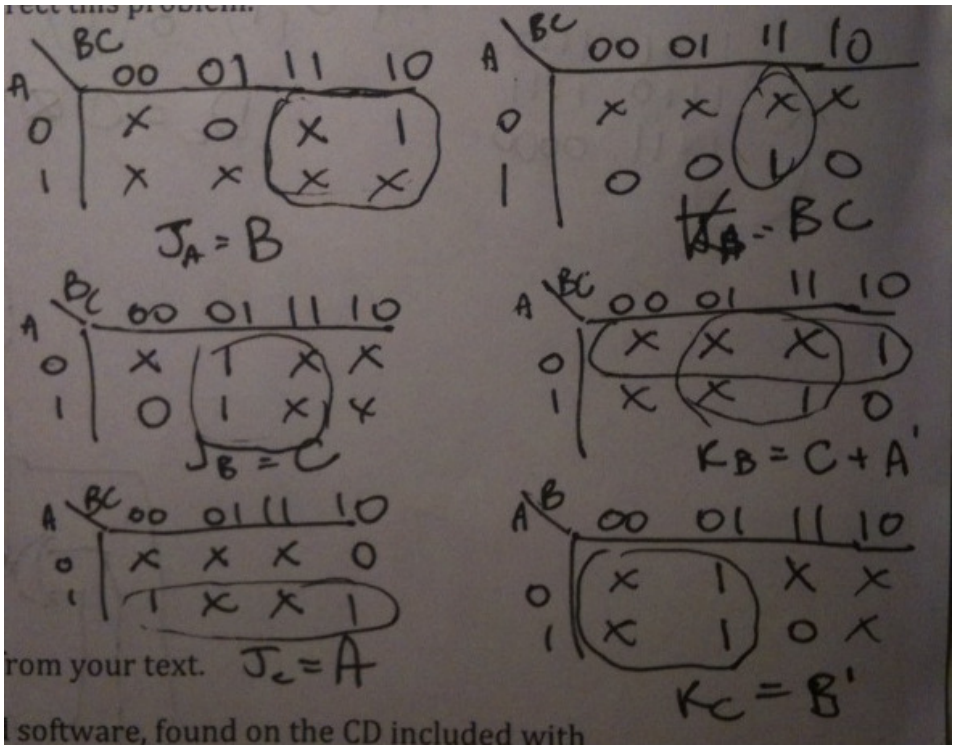
1. Design a four bit binary synchronous counter with D flip-flops and logic gates.

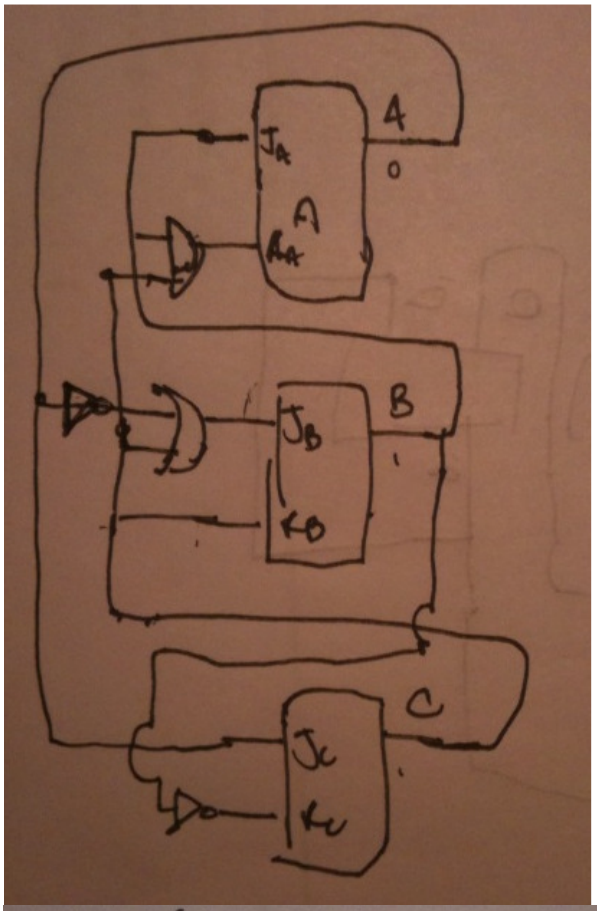




2. Design a counter which cycles through the binary sequence (1,2,4,5,6,7) using J/K flip-flops. Show that when states 000 and 011 are used as don't care statements the counter may not operate properly. Suggest how to correct this problem.







State transition during unknown state values

000 -> 011

011 -> 101

Force unknown states to state 001 or create an error_state output