EECE256 Assignment 6

1. Design a four bit binary synchronous counter with D flip-flops and logic gates.

2. Design a counter which cycles through the binary sequence (1,2,4,5,6,7) using J/K flip-flops. Show that when states 000 and 011 are used as don't care statements the counter may not operate properly. Suggest how to correct this problem.

3. Do questions 6.4, 6.8, 6.16, 6.26, and 6.34* from your text.

* Question 6.34 requires the use of synapticad software, found on the CD included with your text.