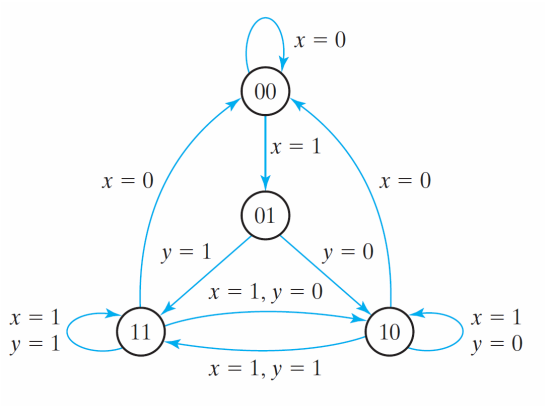
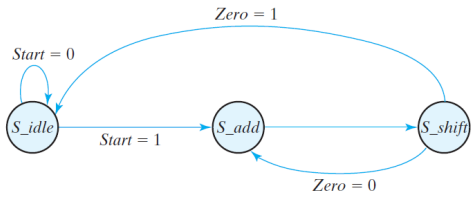
EECE256 Assignment 8

1. Construct a block diagram and ASMD chart for a digital system which counts bikes going in each direction. Two air pressure based sensors are placed side by side, and the corresponding signals, L-Sensor and R-Sensor, transition from 0 to 1 when a bike goes past. A bike going left will first cause an L signal, then an R, while a bike going right will cause an R followed by an L. If the first signal isn't followed by the expected second signal then it shouldn't count the bike, but should return to the reset state. Datapath consists of two counters, one for each direction, which receive a count signal generated by your controller. Assume that only one bike will ride over the sensor at a time.

2. Draw the ASM chart for the following state diagram. Write and verify the equivalent verilog model.



3. Design the binary multiplier controller shown below using multiplexors, a decoder, and a register.



(a)

State Transition		Register Operations
From	To	
S_idle		Initial state
S_idle	*S_add*	$A <= 0, C <= 0, P <= dp\_width$
S_add	*S_shift*	$P <= P - 1$ if ($Q[0]$) then ($A <= A + B, C <= C_{out}$)
S_shift		shift right $\{CAQ\}, C <= 0$

(b)

4. Questions 8.7 (without HDL), 8.9, 8.16, 8.30, 8.31