Registers and Counters

Chapter 6

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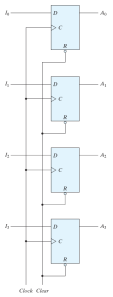
Topics

- Registers
- Shift Registers
- Ripple Counters
- Synchronous Counters
- Other Counters
- HDL

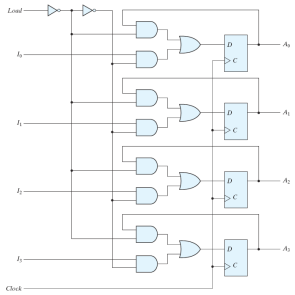
Registers & Counters Overview

- Register
  - Group of flip-flops
  - n-bits (1 per flip-flop)
  - n-bits of binary
- Counter
  - Register with a fixed function

4-bit register



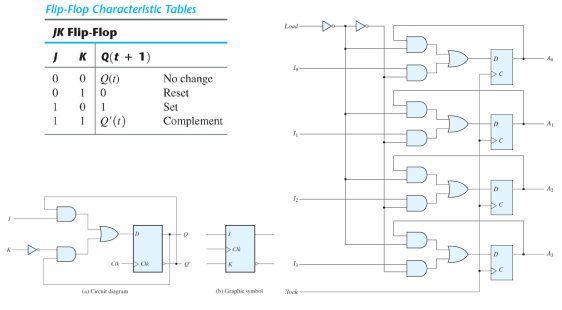
Parallel Load



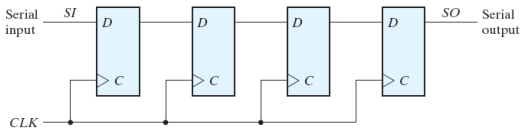
Flip-Flop Characteristic Tables

JK Flip-Flop

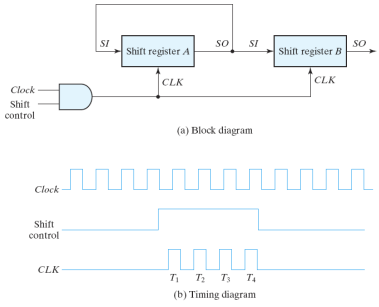
J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement



Shift Registers



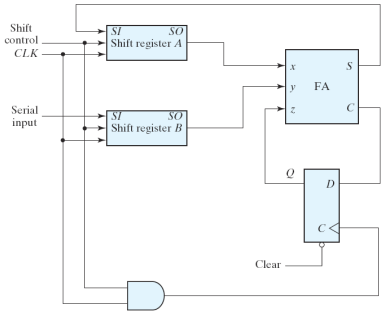
Serial Transfer



Serial Transfer Example

Timing Pulse	Shift Register *A*				Shift Register *B*			
Initial value	1	0	1	1	0	0	1	0
After T_1	1	1	0	1	1	0	0	1
After T_2	1	1	1	0	1	1	0	0
After T_3	0	1	1	1	0	1	1	0
After T_4	1	0	1	1	1	0	1	1

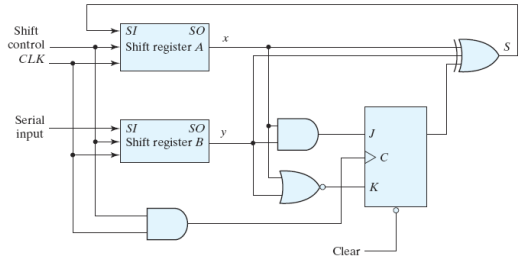
Serial Adder



State Table

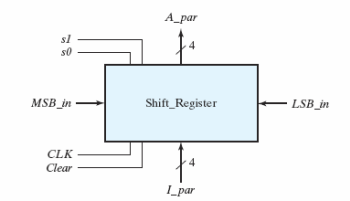
Present State	Inputs		Next State	Output	Flip-Flop Inputs	
Q	x	y	Q	S	J_Q	K_Q
0	0	0	0	0	0	X
0	0	1	0	1	0	X
0	1	0	0	1	0	X
0	1	1	1	0	1	X
1	0	0	0	1	X	1
1	0	1	1	0	X	0
1	1	0	1	0	X	0
1	1	1	1	1	X	0

Serial Adder Circuit

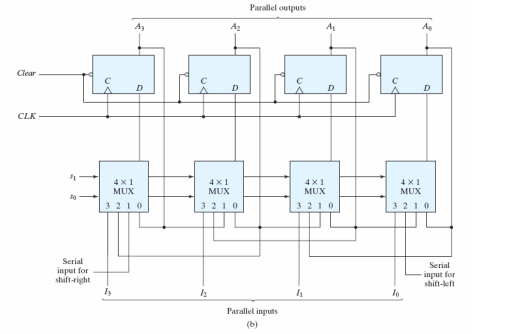


Universal Shift Register

- Clear
- Clock
- Shift Right
- Shift Left
- Parallel load
- n Parallel Outputs
- Control



Universal Shift Register

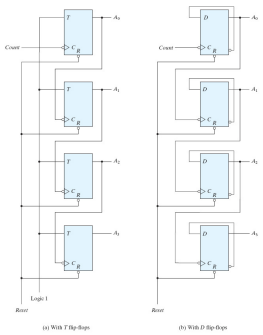


Shift Register Controls

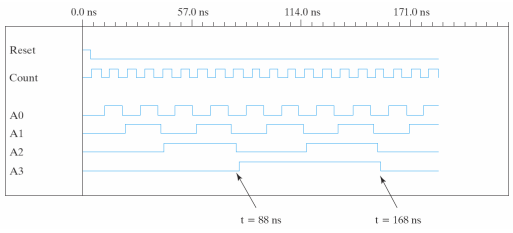
Mode Control

s_1	s_0	Register Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

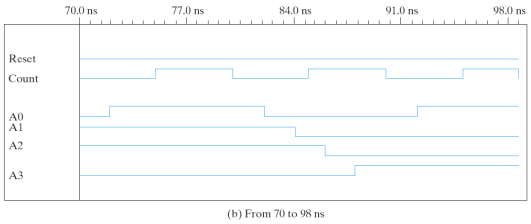
Ripple Counters



Ripple Counter Timing Diagram



Close Up

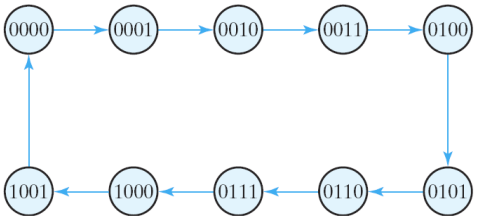


(b) From 70 to 98 ns

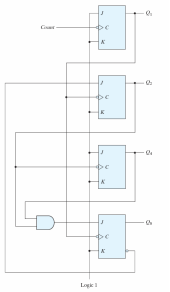
Counting Sequences

A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0

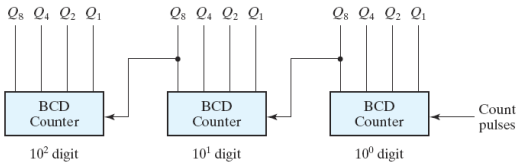
State Diagram of BCD counter



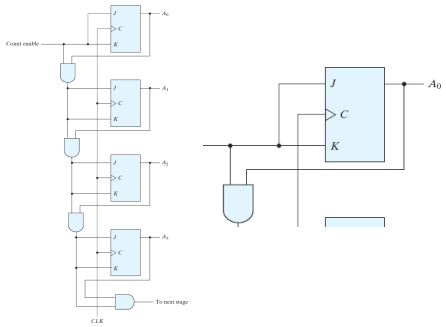
BCD Ripple Counter



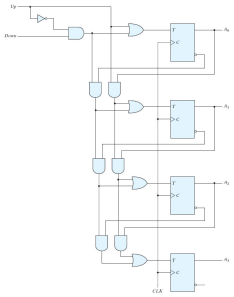
Three decade counter

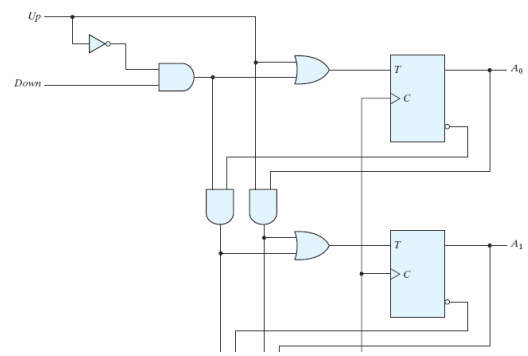


Synchronous Counters



Binary Up Down Counter

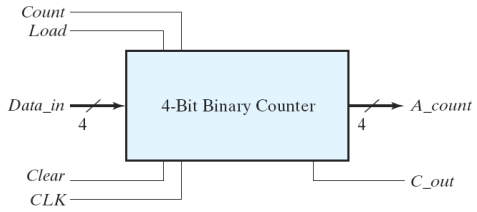


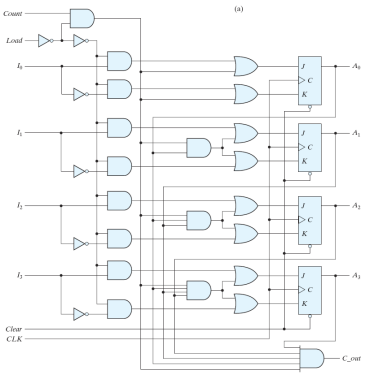


BCD Synchronous Counter State Table

Present State				Next State				Output	Flip-Flop Inputs			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1	y	TQ_8	TQ_4	TQ_2	TQ_1
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

4-bit Binary Counter

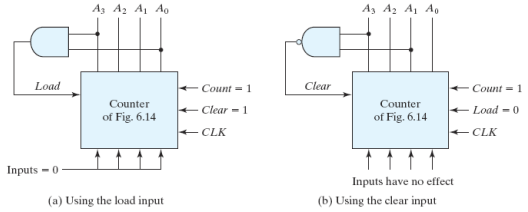




Function of the Counter

Clear	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change

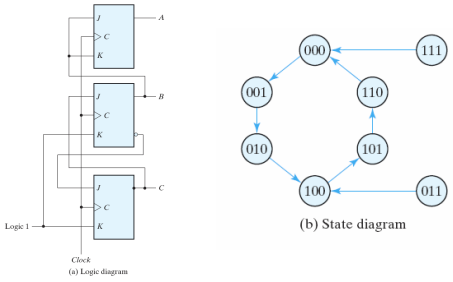
BCD Counter



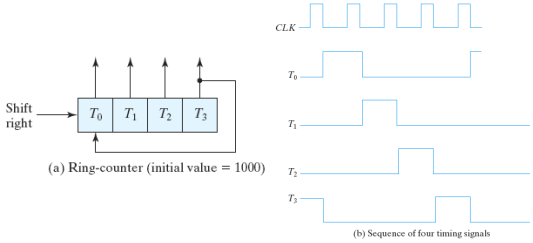
Other types of Counters

Present State			Next State			Flip-Flop Inputs					
A	B	C	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X

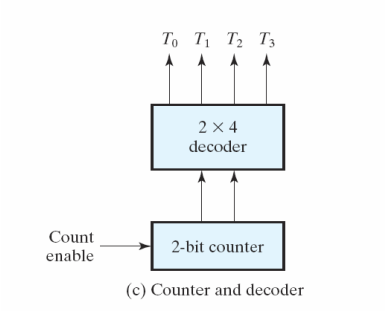
Counter with unused states



Ring Counter

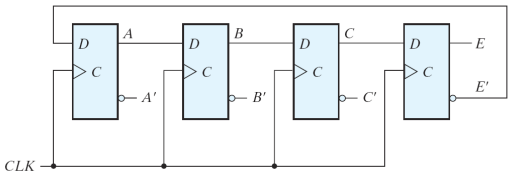


Ring Counter



(c) Counter and decoder

Johnson Counter



(a) Four-stage switch-tail ring counter

Johnson Counter

Sequence number	Flip-flop outputs				AND gate required for output
	A	B	C	E	
1	0	0	0	0	$A'E'$
2	1	0	0	0	AB'
3	1	1	0	0	BC'
4	1	1	1	0	CE'
5	1	1	1	1	AE
6	0	1	1	1	$A'B$
7	0	0	1	1	$B'C$
8	0	0	0	1	$C'E$

(b) Count sequence and required decoding

HDL Binary Counter

```
module Binary_Counter_4_Par_Load (

  output reg [3:0]      A_count,  // Data output
  output    C_out,      // Output carry
  input [3:0]           Data_in,   // Data input
  input      Count,     // Active high to count
     Load, // Active high to load
     CLK,  // Positive edge sensitive
     Clear // Active low
);

assign C_out = Count & (~Load) & (A_count == 4'b1111);
always @ (posedge CLK, negedge Clear)
  if (~Clear)           A_count <= 4'b0000;
  else if (Load) A_count <= 4'b0000;
  else if (Count)       A_count <= A_count + 1'b1;
  else       A_count <= A_count;              // redundant statement
endmodule
```

Registers & Counters Review

- Register
  - Group of flip-flops
  - D, J/K,T
- Counter
  - Register with a fixed function
  - Ripple Counter
  - Parallel Load
  - Ring Counter
  - Johnson Counter