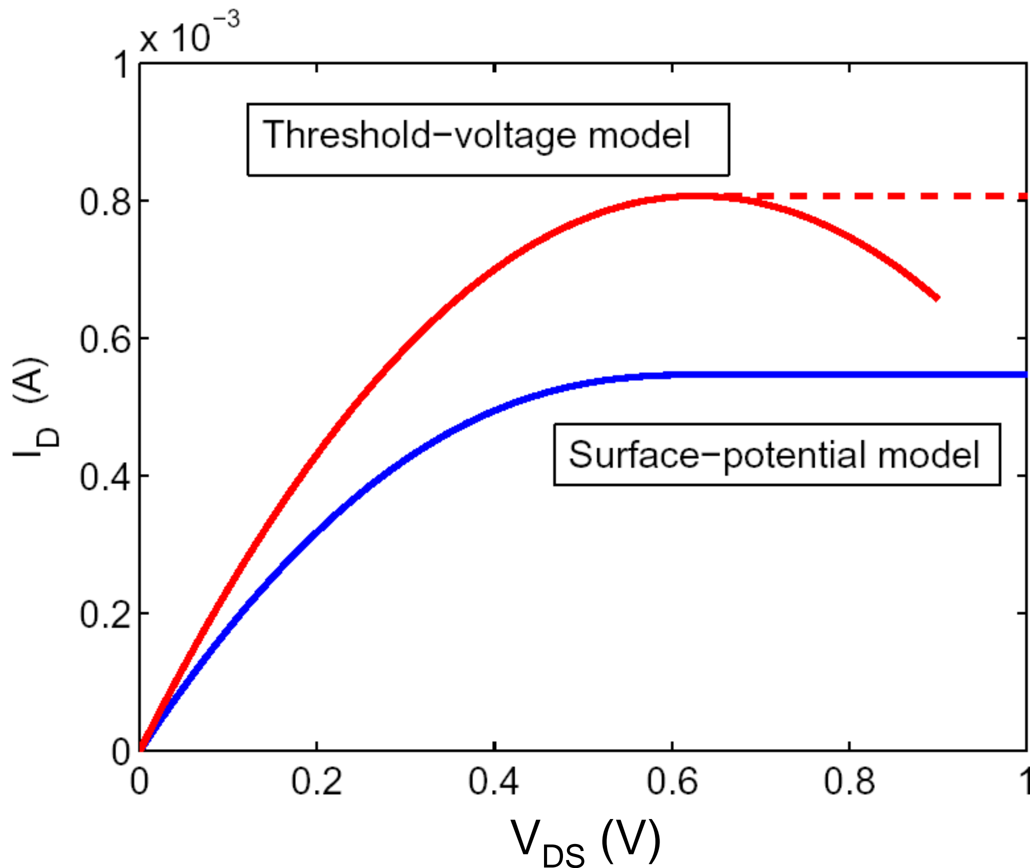
MOSFETs for digital logic

LECTURE 20

- Summary of PSP and SPICE models
- Threshold voltage
- Body-effect coefficient
- Effective mobility
- Effect of velocity saturation on I-V characteristic
- Sub-threshold current
- CMOS digital logic

Sec. 10.4.3

Comparison of PSP and SPICE



$$I_D = ZC_{ox}\left[V_{GS} - V_T - m\frac{V_{DS}}{2}\right] \cdot \mu_{\text{eff}}\frac{V_{DS}}{L}$$

Differentiate wrt V_{DS} to find V_{DSsat}

$$V_{DS} \equiv V_{DSsat} = \boxed{}$$

Substitute into I_D to get I_{Dsat}

$$I_{Dsat} = \frac{Z}{L}C_{ox}\mu_{\text{eff}}\boxed{}$$

- SPICE LEVEL 1 has the correct form for the drain characteristic, but is not very accurate.
- However, its use of V_T is very helpful in formulating a simple algorithm for MOSFET operation.

MOSFET model summary

PSP:

- Gradual Channel Approximation - enables solution of Poisson to get Q_s
- Use Q=CV to get another expression for Q_s
- Equate and get implicit expression for φ_s (V_{GB}, V_{DB}, V_{SB})
- Charge Sheet Approximation - no $\Delta V(y)$ across channel - φ_s due to Q_b - use DA
- DDE for I_D
- Predicts exponential-dependence on V_{GB} at low bias and weaker dependence at higher V_{GB}.
- It is a model for all conditions

SPICE:

1. Assumes channel is strongly inverted everywhere. This is not true at the drain for moderate and high V_{DS}, so the model only works in the triode regime ($V_{DS} < V_{GS} - V_T$).
2. Patch-up the model by assuming I_D saturates at the `breakdown' point.
3. LEVEL 1 assumes $v_d = \mu E_x$. So I_D is overestimated at high E_x.
4. LEVEL 49 limits v_d to v_{dsat}, so it gives more a more realistic I_D.
5. I_D(SPICE) > I_D(PSP) because of strong inversion assumption.
6. SPICE gives us V_T - the `long-channel' threshold voltage, which is a widely used metric.
7. Our SPICE models only work for $V_{GS} > V_T$, i.e., when the FET is ON.

Sec. 10.4.2

Threshold voltage

$$V_T = V_{fb} + 2\phi_B + \gamma\sqrt{2\phi_B + V_{SB}}$$

$$-V_{fb} = V_{bi}^{\mathrm{MOS}} = \frac{\Phi_S - \Phi_G}{q}$$

$$n_i e^{-q\phi_B/kT} = \frac{n_i^2}{N_A}$$

$$\gamma = \sqrt{2q\epsilon_s N_A}/C_{ox}$$

V_T is the V_{GS} at which the surface is strongly inverted at the source end of the channel,

i.e.,

$$\psi_s(0) =$$

Information on CMOS65 process:

$V_T =$

$t_{ox} = 1.7\,\mathrm{nm}$;

$\epsilon_{ox} = 3.9\epsilon_0$;

$N_A = 2.6 \times 10^{18}\,\mathrm{cm}^{-3}$;

$\mu_{\mathrm{eff}} = 600\,\mathrm{cm}^2(\mathrm{Vs})^{-1}$;

$v_{sat} = 12 \times 10^6\,\mathrm{cm/s}$;

Exercise: Evaluate V_T

Sec. 10.4.4

Body-effect coefficient

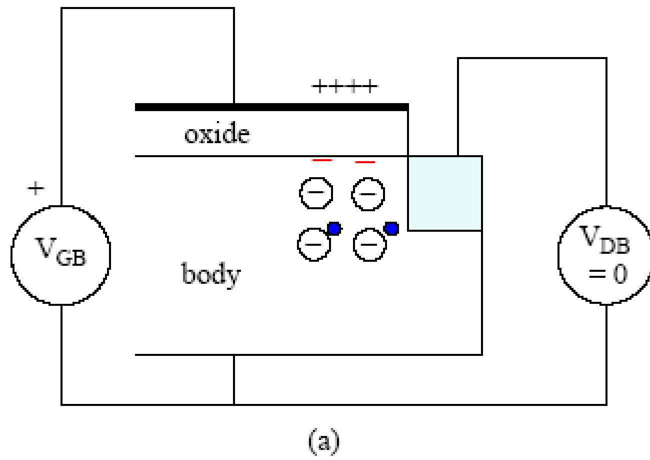
m came from the binomial expansion of the drift part of the PSP expression for drain current.

Effectively, it s for the fact that a change in charge on the gate does not translate into an equal change in charge in the channel, because there is also some charge change in the body.

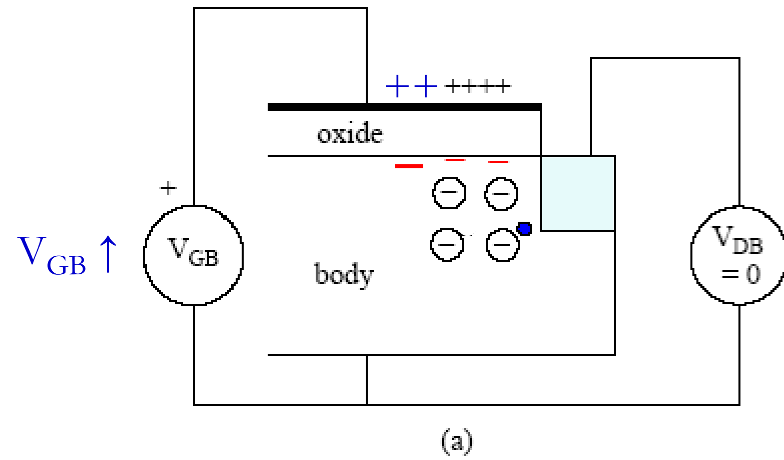
$$I_D = ZC_{ox}\left[V_{GS} - V_T - m\frac{V_{DS}}{2}\right]\cdot\mu_{\text{eff}}\frac{V_{DS}}{L}$$

$$m = 1 + \frac{\gamma}{2\sqrt{2\phi_B + V_{SB}}}$$

$$\gamma = \sqrt{2q\epsilon_s N_A}/C_{ox}$$



(a)



(a)

$$\Delta Q_G + \Delta Q_n + \Delta Q_b = 0$$

$$\Delta Q_G + \Delta Q_n(1 + \frac{\Delta Q_b}{\Delta Q_n}) = 0$$

What is m?

Sec. 10.3.2

Effective mobility

$$I_D = ZC_{ox}\left[V_{GS} - V_T - m\frac{V_{DS}}{2}\right]\cdot\mu_{\text{eff}}\frac{V_{DS}}{L}$$

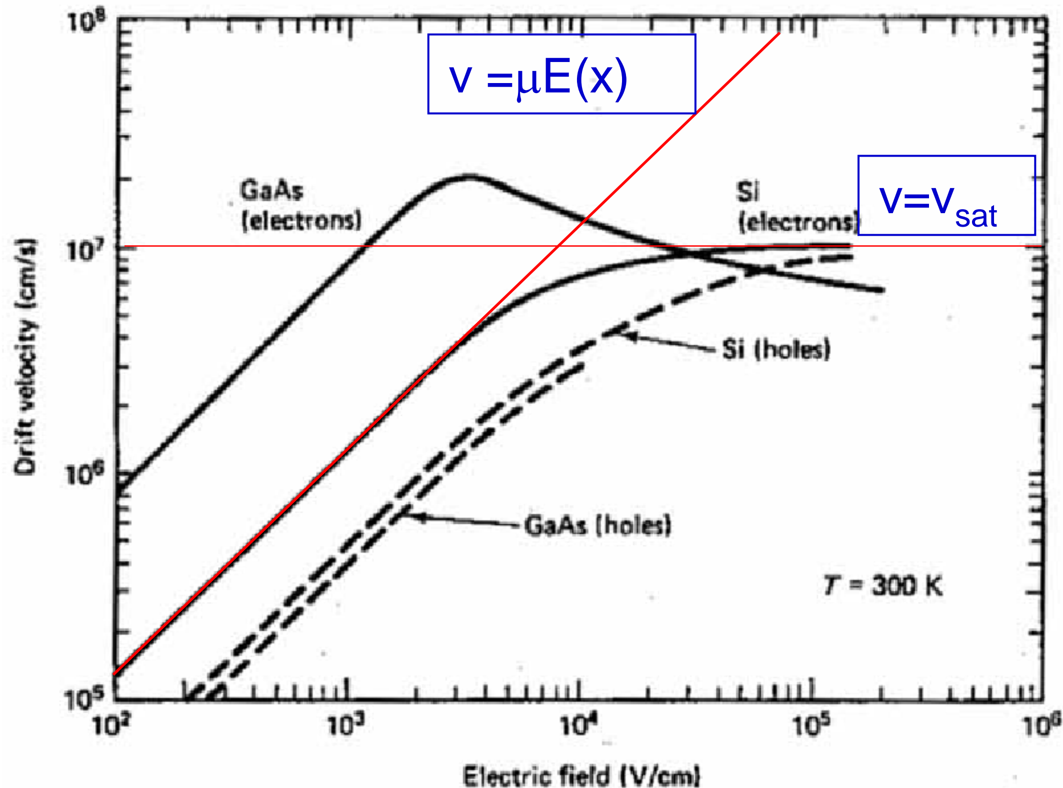
The effective mobility in the channel is different from the low-field electron mobility in the bulk because of 2 reasons.

1.

2.

Secs. 5.4,10.4.5

SPICE Level 49: allowing for v_{sat}



Combining the velocities:

$$v(x) = \frac{1}{\frac{1}{\mu E(x)} + \frac{1}{v_{sat}}}$$

Substitute for v_d in:

$$I_D = ZC_{ox}\left[V_{GS} - V_T - mV_{CS}(x)\right].v_d(x)$$

Use:

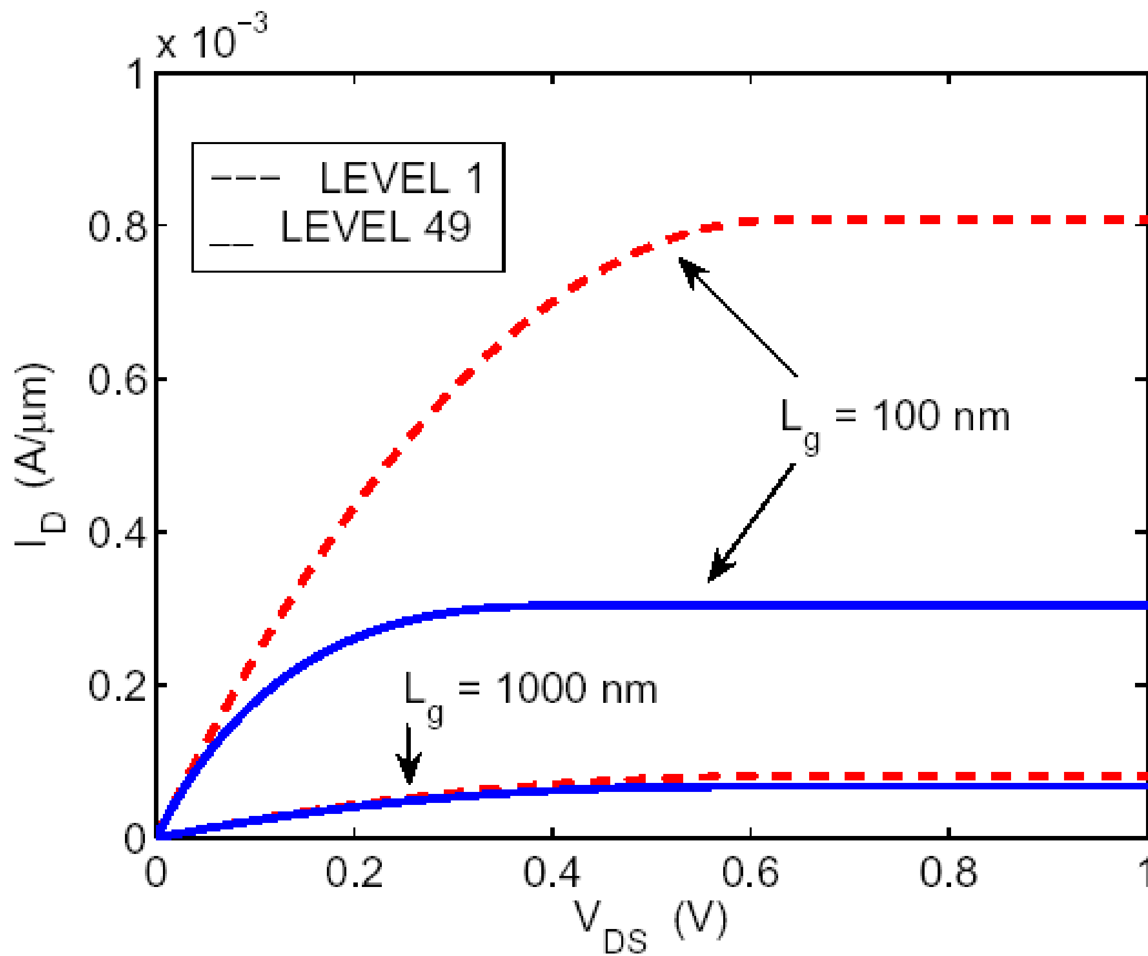
$$|\mathcal{E}_x| = dV_{CS}(x)/dx$$

Integrate:

$$I_D = ZC_{ox}\left[V_{GS} - V_T - m\frac{V_{DS}}{2}\right].\mu_{\text{eff}}\frac{V_{DS}}{L + (\mu_{\text{eff}}V_{DS}/v_{\text{sat}})}$$

Sec. 10.4.5

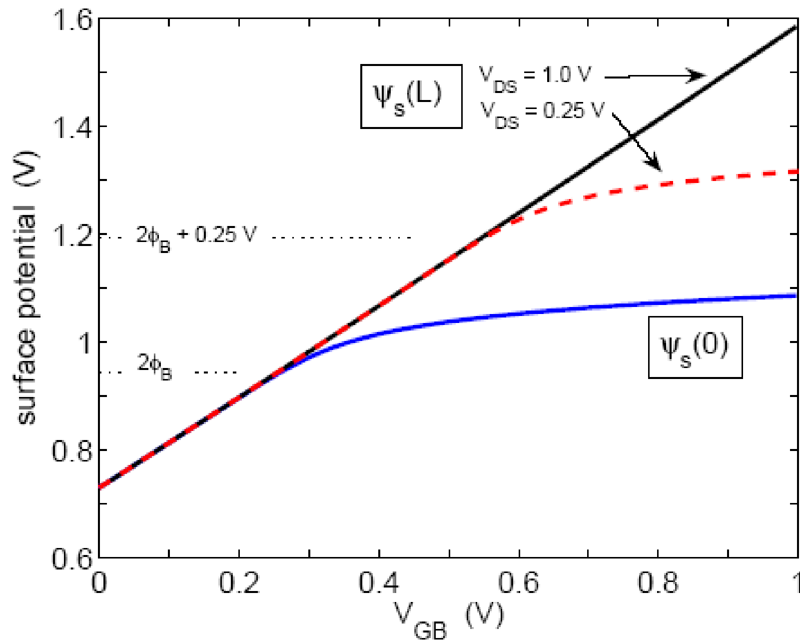
Comparison of SPICE Levels 1 and 49

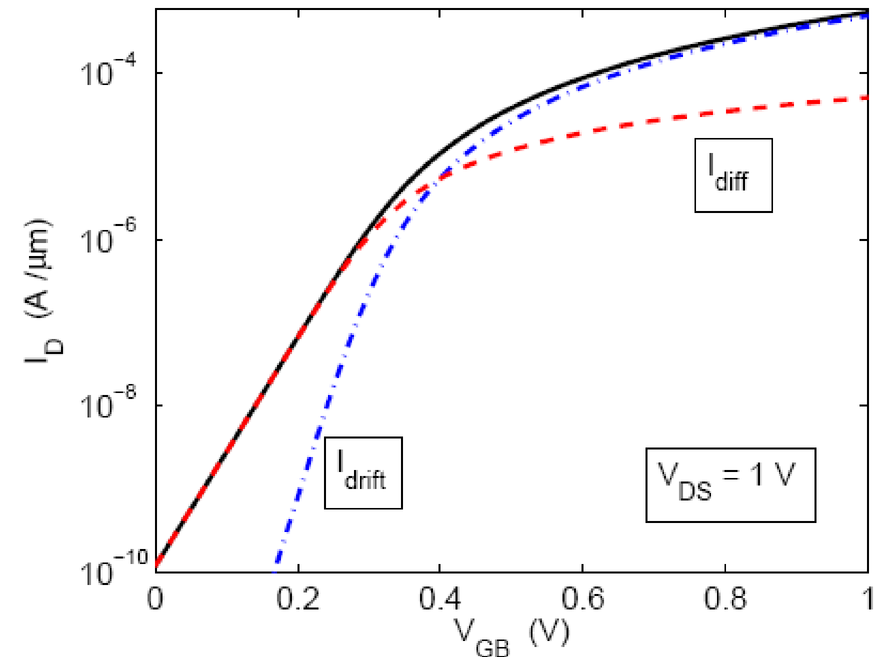


What is the conclusion from this?

Secs. 10.5, 13.1.10

Sub-threshold current





$$I_D = \frac{Z}{L}\mu_{\rm eff}\left(\frac{k_BT}{q}\right)^2 C_{ox}(m-1) \qquad \left\{1 - e^{-V_{DS}/V_{\rm th}}\right\}$$

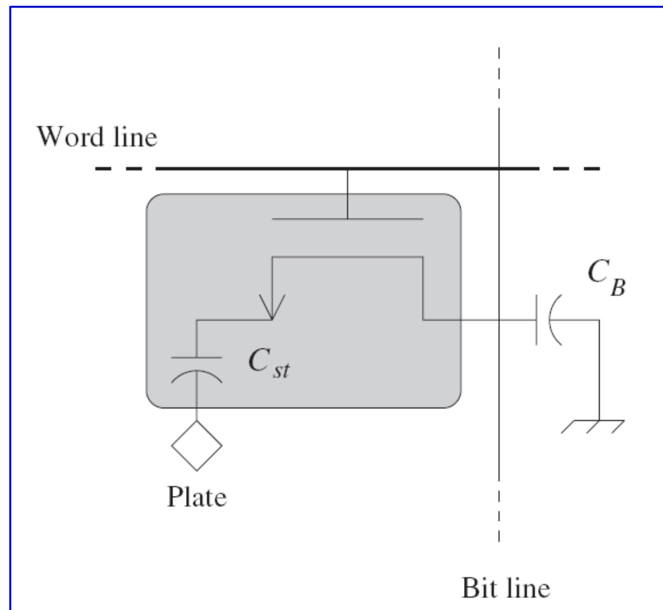
Inverse sub-threshold slope is the gate bias required to reduce $I_{D,\ subT}$ by 10

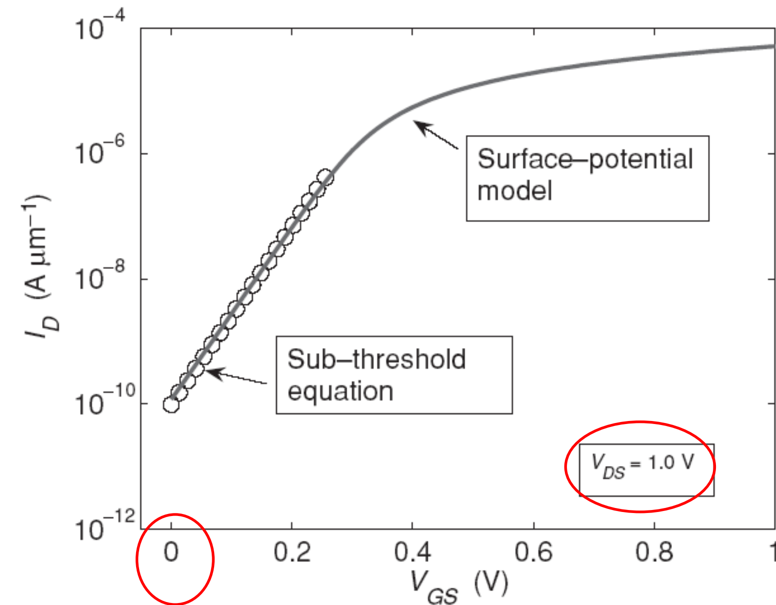
$$S = \left(\frac{\partial \log_{10} I_D}{\partial V_{GS}}\right)^{-1} = 2.303 m\, V_{\rm th}$$

What does V_T have to be for $I_{OFF}/I_{ON}=10^{-4}$?

Sec. 13.0

OFF current and DRAM storage time

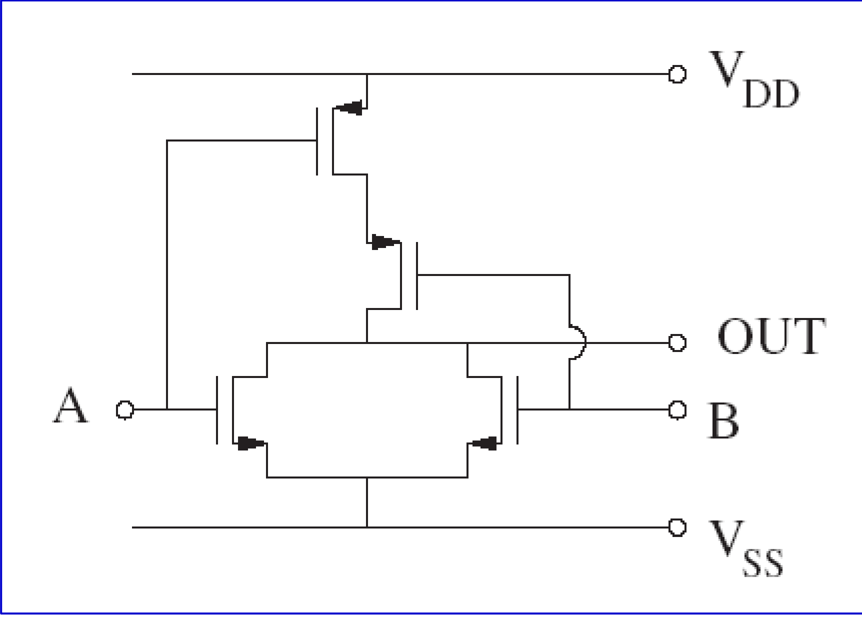




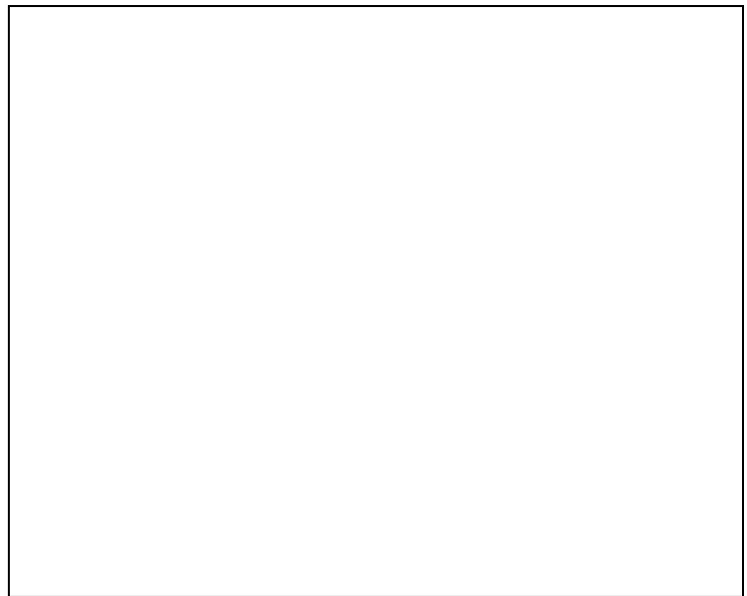
How long will it take to discharge C_{st} =1pF to V_{DS}= 0.5V when the Bit line is LO and the NFET (Z=100 nm) is supposed to be OFF?

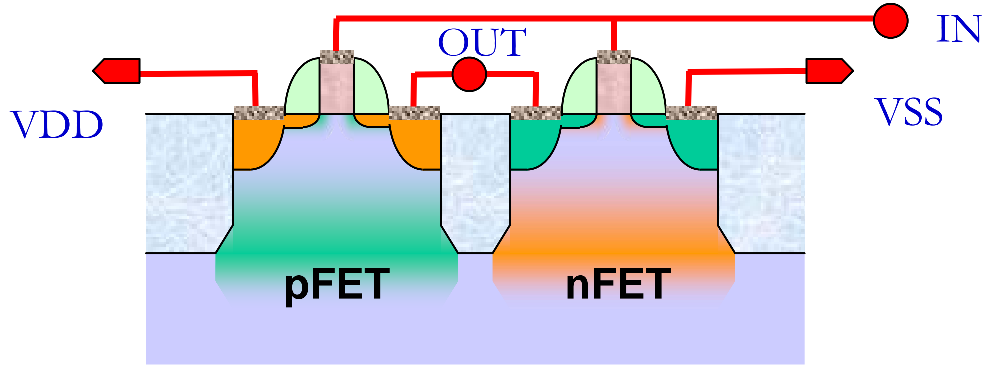
Chap. 13

Si CMOS: why is it dominant for digital?



4 reasons:

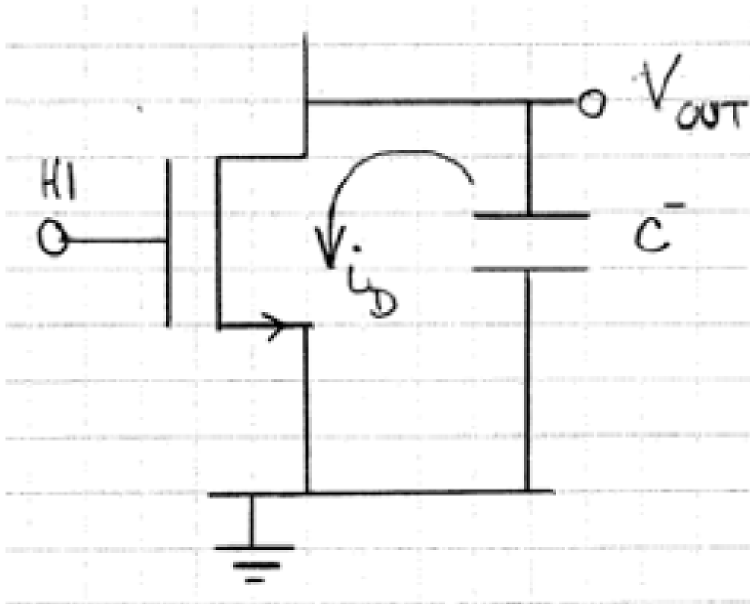


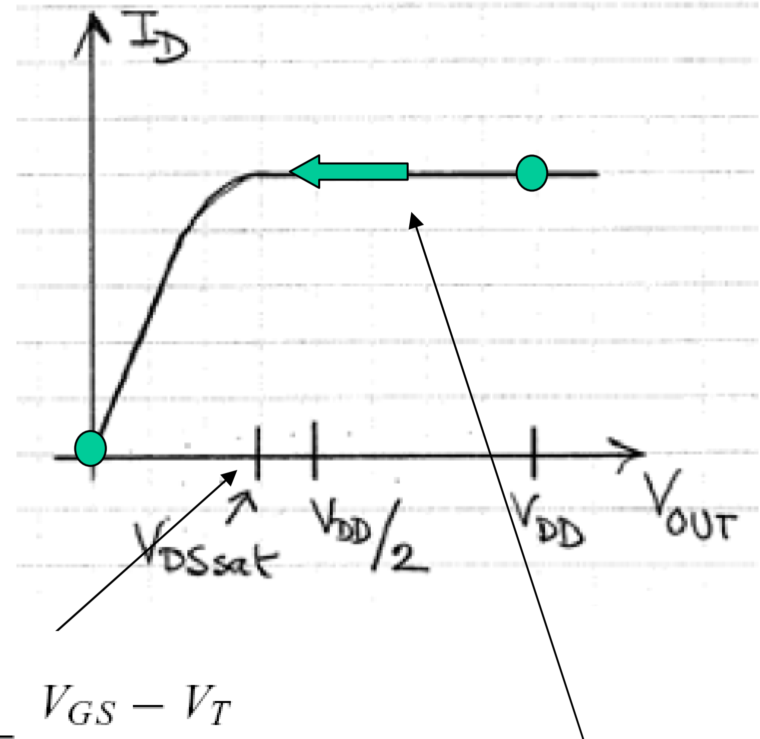


Example of small footprint

Sec. 13.0

Logic speed is about Q and I





$$\tau = \frac{C\Delta V}{I}$$

$$V_{DS} \equiv V_{DSsat} = \frac{V_{GS} - V_T}{m}$$

$$I_{Dsat} = \frac{Z}{L} C_{ox} \mu_{\text{eff}} \frac{(V_{GS} - V_T)^2}{2m}$$

For about 40 years (1963-2003), steady improvements in speed were accomplished by:

- reducing L and V_T to increase I_{ON}
- reducing L and Z to decrease C_{FET}
- can these trends continue?