High performance CMOS: gate-stack engineering

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LECTURE 22

- the effect of Cox on leakage and ON currents
- high-k dielectrics
- tunneling through the oxide
- the importance of electron affinity
- metal gates

ON current:

$$I_{Dsat} = ZC_{ox}(V_{GS} - V_T) \cdot v_{sat} \frac{\sqrt{1 + 2\mu_{eff}(V_{GS} - V_T)/(mv_{sat}L)} - 1}{\sqrt{1 + 2\mu_{eff}(V_{GS} - V_T)/(mv_{sat}L)} + 1}$$

Break this down into charge and velocity.

A high C_{ox} is needed to get more charge in the channel.

OFF Current:

A high C_{ox} is needed to get a steeper inverse sub-threshold slope

$$S = \left(\frac{\partial \log_{10} I_D}{\partial V_{GS}}\right)^{-1} \equiv 2.303 m V_{\rm th}$$

$$m(0) = 1 + \frac{\gamma}{2\sqrt{2\phi_B + V_{SB}}} \equiv 1 + \frac{C_b(0)}{C_{ox}}$$

Relation between m and C_b(0)

$$[0.3] \quad \text{From (10.43)} \quad m = 1 + \frac{v}{2\sqrt{24g} + V_{SB}} \quad \text{ordere } S = \sqrt{2q} \frac{c_s}{N_A}$$

$$C_b = \frac{c_s}{W} = \frac{c_s}{\sqrt{2g} \frac{24g}{2} + V_{SB}} \quad @ 2t_s = 24g \rightarrow C_b = \frac{1}{\sqrt{2}} \frac{c_s}{\sqrt{24g}} \frac{N_A}{24g}$$

$$= \frac{1}{2} \sqrt{\frac{2s}{24g}} \frac{N_A}{24g}$$

$$\therefore S C_{SC} = 2 C_b \sqrt{24g}$$
and $m = 1 + \frac{C_b}{C_{SC}}$ as per (10.36), pronded $2t_s = 24g$,
$$\frac{C_b - \frac{1}{24g}}{\frac{24g}{24g}} \frac{1}{24g}$$

$$\frac{V_{SB} = 0}{V_{SB}} = 0.$$

The C_{ox} dilemma: 2

Leakage current:

$$C_{ox} = \frac{\mathcal{E}_{ox}}{t_{ox}}$$

There's a limit to how far t_{ox} can be reduced before channel-gate leakage occurs



High-k dielectrics



- High C_{OX} needed for I_D and S
- High t_{OX} needed to reduce gate leakage
- Resolve conflict by increasing ε

Dielectric	Dielectric constant (bulk)
Silicon dioxide (SiO ₂)	3.9
Silicon nitride (Si ₃ N ₄)	7
Aluminum oxide (Al ₂ O ₃)	~ 10
Tantulum pentoxide (Ta_2O_5)	25
Lanthanum oxide (La ₂ O ₃)	~21
Gadolinium oxide (Gd ₂ O ₃)	~12
Yttrium oxide (Y2O3)	~15
Hafnium oxide (HfO ₂)	~ 20
Zirconium oxide (ZrO ₂)	~23

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Tunneling through the oxide



Electron energy

Sec. 5.7.2

Solutions for $\psi \psi^*$



Emphasizing the reduction in $\psi \psi^*$

Sec. 5.7.2



Figure 5.9 Redrawing of the probability density from Fig. 5.8 The logarithmic scale emphasizes the small ($\approx 10^{-8} \text{ m}^{-1}$) probability density of electrons tunneling from region 1.



Probability Density Current

$$\begin{split} \frac{dP}{dt} &= \Psi^* \frac{\partial \Psi}{\partial t} + \Psi \frac{\partial \Psi^*}{\partial t} \\ &= \frac{1}{i\hbar} \left[\Psi^* (i\hbar \frac{\partial \Psi}{\partial t}) + \Psi (i\hbar \frac{\partial \Psi^*}{\partial t}) \right] \end{split}$$

What does the flow of P mean ?

The time-dependent Schrödinger Wave Equation is

$$i\hbar\frac{\partial\Psi}{\partial t}=-\frac{\hbar^2}{2m^*}\nabla^2\Psi+U\Psi$$

$$\frac{dP}{dt} = -\frac{i\hbar}{2m^*} \nabla \cdot \left[\Psi \nabla \Psi^* - \Psi^* \nabla \Psi\right]$$
$$\equiv -\nabla \cdot \vec{J}_P$$

Do you recognize this as a Continuity Equation ?

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Transmission Probability: Definition

$$\frac{dP}{dt} = -\frac{i\hbar}{2m^*} \nabla \cdot \left[\Psi \nabla \Psi^* - \Psi^* \nabla \Psi\right]$$
$$\equiv -\nabla \cdot \vec{J_P}$$

1. For the channel:

$$\psi_1 = Ae^{ik_1y} + Be^{-ik_1y}$$

2. Do the derivatives and the conjugates:

$$J_{P,A} = \frac{\hbar k_1}{m_1^*} |A|^2$$
$$J_{P,F} = \frac{\hbar k_3}{m_3^*} |F|^2$$

What do these mean?

3. Define the Transmission Probability:

$$T(E) = \frac{k_3}{k_1} \frac{m_1^*}{m_3^*} \frac{|F|^2}{|A|^2}$$
$$\equiv \frac{v_{k,3}}{v_{k,1}} \frac{|F|^2}{|A|^2},$$

What is the interpretation of this ?

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Solve for F and A:

Sec. 5.7.2

 $4m_1k_3/m_3k_1$

 $T = \frac{1}{(1 + k_3 m_1 / k_1 m_3)^2 \cosh^2(k'_2 d) + (k'_2 m_1 / k_1 m_2 - k_3 m_2 / k'_2 m_3)^2 \sinh^2(k'_2 d)}$



Sec. 13.1.6

Silica vs. Hafnia: properties



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	ϵ_r	t_{ox}	χ	m^*
		(nm)	(eV)	(m_0)
Silica	3.9	2.3	0.9	0.3
Hafnia	$5\epsilon_{r,\mathrm{silica}}$	$t_{ox}\epsilon_{r,\mathrm{hafnia}}/\epsilon_{r,\mathrm{silica}}$	2.9	0.1
Silicon	-	-	4.1	0.91

The importance of electron affinity



Figure 13.8: Ratio of tunnel current in a high-k dielectric to that in silica as a function of the electron affinity of the high-k dielectric. The high-k dielectric is taken to have a relative permittivity that is 4 times that of silica. The top curve is for an improvement in C_{ox} of 100%, and the bottom curve is for an improvement of 50%. The parameter values are as given in the caption to Fig. 5.9, unless otherwise stated. $(E_{C,Si} - E_F)$ was taken to be 50 meV.

Is it possible to reduce I_{leak} and improve I_{ON} ?

Sec. 13.1.6

The new gate stack

45nm High-k + Metal Gate Strain-Enhanced CMOS Transistors

Chris Auth Logic Technology Development, Intel Corp., Hillsboro, OR, U.S.A.



Figure 3: TEM of High-k/Metal gate stack

Guess what Intel is doing



Figure 5: TEMs of High-k + Metal Gate NMOS (left) and PMOS (right) transistors

Threshold voltage

$$V_T \equiv V_{GS}^T = V_{fb} + 2\psi_B + \frac{1}{C_{ox}}\sqrt{2\epsilon_S q N_A (2\psi_B + V_{SB})}$$

What if N_A were greatly reduced?



- If V_T controlled by metal, perhaps can use undoped Si substrate.
- This would remove the problem of dopant fluctuations.
- But what about self-alignment?

Another reason for metal gates



The finite conductivity of the poly-gate results in band bending in the gate.

$$V_{GB} - V_{fb} = \psi_{\text{poly}} + \psi_{ox} + \psi_s$$

How does this affect V_T ?